DESCRIPTION

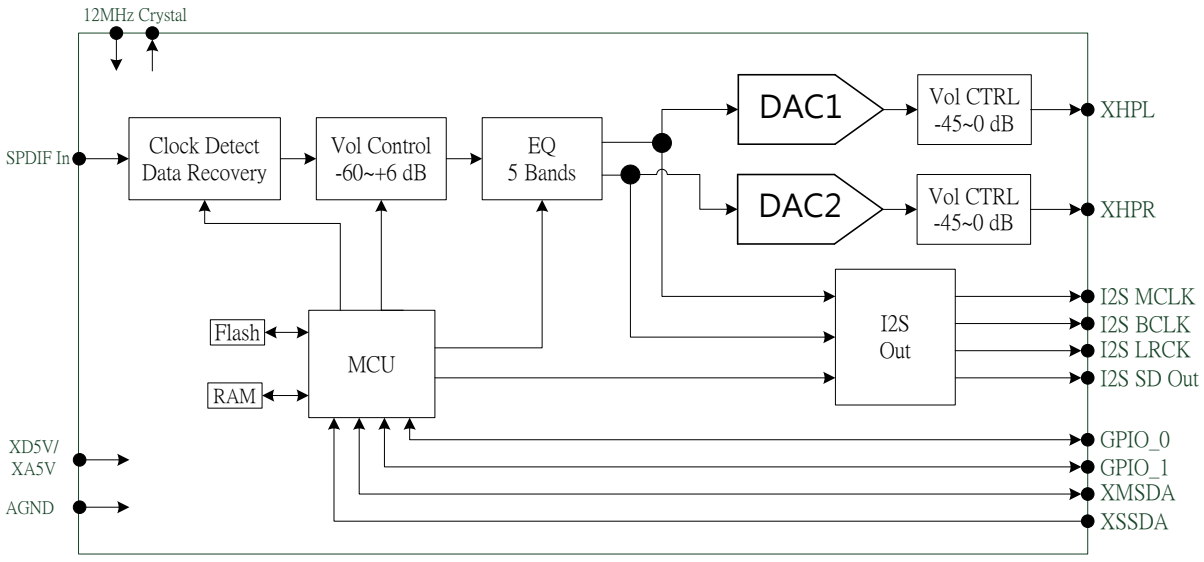
The CM7037 is a S/PDIF in receiver to convert the audio data to I2S and analog out. The input audio format of SPDIF in signal can be detected automatically and convert to I2S and analog out.

The CM7037 only supports standard IEC60958, PCM Audio data. If the data is non PCM, there will be no output for the I2S and analog out.

FEATURES

- S/PDIF input signal support up to 192KHz/24bits
- Automatically detect PCM/non PCM Audio data
- I2C interface for external MCU to read audio format status and control programmable function pin
- 2 channel capless headphone output
- 2 channel I2S output
- Support 5 bands EQ
- Integrate 8051 MCU1 I2C master, 1 I2C slave, 1 SPI master, 6GPIOs
- Integrate 3 PWM LED drivers

BLOCK DIAGRAM



Release notes

Revision	Date	Description
0.90	2021/12/08	- Preliminary release
0.91	2021/12/17	- Modify Pin Description
1.00	2022/08/23	- Formal release
1.10	2025/06/30	- Modify Electrical Characteristics

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1 Description and Overview

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2 Ordering Information

Product	Package Marking	Package Type	Transport Media
CM7037	CM7037	QFN-48(5x5mm)	Tray

3 Features

3.1 Integrated 8051 Micro Processor

- Embedded 8051 micro-processor
- Communicate with external peripheral devices(I2C, SPI, GPIO, etc.)
- The MCU speed is programmable from 3.072 to 65.536 MHz

3.2 Control Interface

- 1 Master I2C control interface to communicate with external devices or EEPROM, the master I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 Slave I2C control interface for external MCU communication, the slave I2C speed supports standard mode(100KHz) and fast mode(400KHz)
- 1 SPI master(share with GPIO), supports speed from 0.384 to 24.576 Mb/s
- 6 GPIOs(programmable multi functions I/O)
- 3 PWM LED drivers output share with GPIO

3.3 General

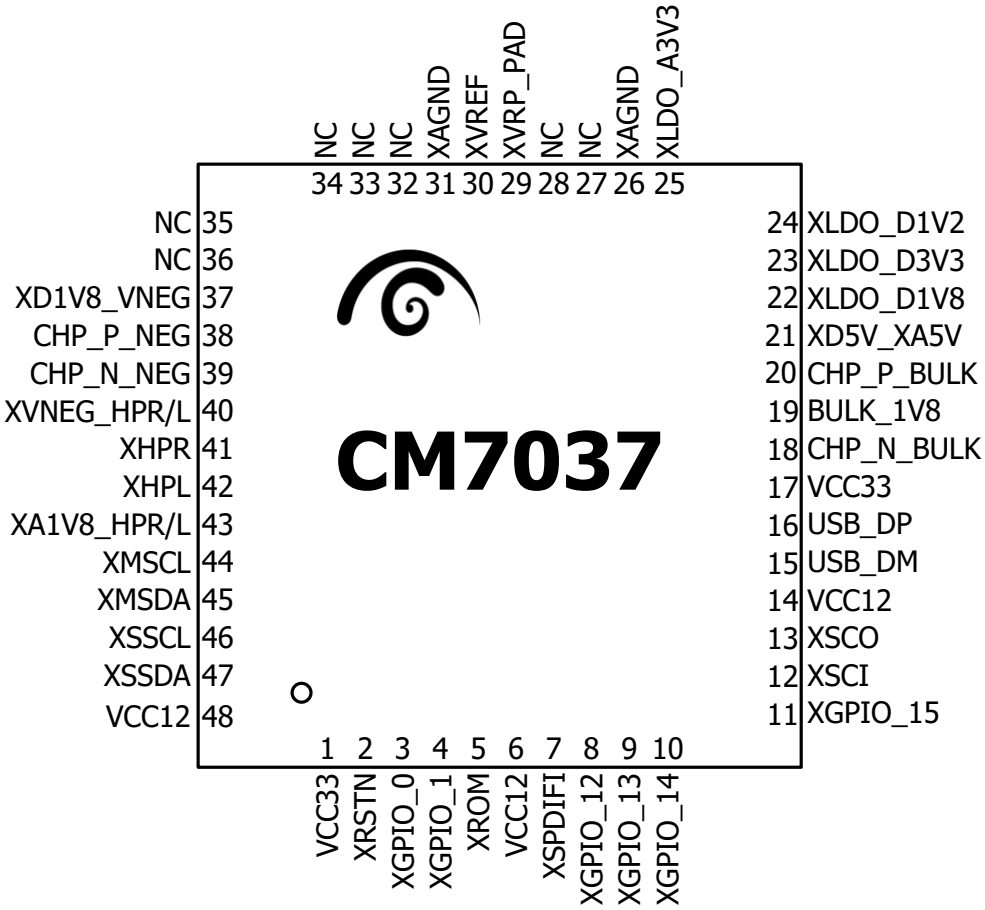
- PCM / non-PCM audio data detection
- Single 5V power supply with embedded 5V to 3.3V regulator.
- 3.3V digital I/O pads with 5V tolerance
- QFN-48 package (5 x 5 mm)

4 Applications

- Digital to analog audio convert
- Set-top box
- A/V receiver
- Multimedia speaker

5 Pin Assignment

5.1 Pin-out Diagram



5.2 I/O Type Description

I/O Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIL	Digital Input with internal pull-down 50K
DIH	Digital Input with internal pull-up 50K
DIOL	Digital Input/Output with internal pull-down 50K
DIOH	Digital Input/Output with internal pull-up 50K
IOU	USB related IO
PWRO	Power output pin
PWRI	Power input pin
GND	Ground related pin

5.3 Pin Description

Pin #	Symbol	I/O	Description
USB 2.0 BUS Interface			
16	USB_DP	IOU	USB 2.0 data positive
15	USB_DM	IOU	USB 2.0 data negative
Power/Ground			
21	XD5V_XA5V	PWRI	Digital/Analog supply power (4.3V~5V) ; Connect to capacitor filter
26	XAGND	GND	Analog ground
31	XAGND	GND	Analog ground
19	BULK_1V8	PWRO	DC to DC 1.8V output, 40mA driving current ; Connect to capacitor filter
37	XD1V8_VNEG	PWRI	DC to DC 1.8V input Input power of negative charge pump ; Connect to capacitor filter
43	XA1V8_HPR/L	PWRI	Analog 1.8V input Positive Power of headphone driver R/L CH ; Connect to capacitor filter
40	XVNEG_HPR/L	PWRO	DC to DC -1.8V output, 10mA driving current ; Connect to capacitor filter
25	XLDO_A3V3	PWRO	LDO 3.3V output, 20mA driving current ; Connect to capacitor filter
23	XLDO_D3V3	PWRO	LDO 3.3V output, 30mA driving current ; Connect to capacitor filter
22	XLDO_D1V8	PWRO	LDO 1.8V output, 20mA driving current ; Connect to capacitor filter
24	XLDO_D1V2	PWRO	LDO 1.2V output, 10mA driving current ; Connect to capacitor filter
17	VCC33	PWRI	VCC 3.3V input Digital supply voltage 3.3V for digital I/O
1	VCC33	PWRI	VCC 3.3V input Digital supply voltage 3.3V for digital I/O
6	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core

14	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
48	VCC12	PWRI	VCC 1.2V input Digital supply voltage 3.3V for digital core
Analog			
30	XVREF	AO	Voltage reference for common mode voltage (~1.5V)
29	XVRP_PAD	AO	Voltage reference for DAC (~3.1V)
20	CHP_P_BULK	AO	Charge pump positive output of DC to DC
18	CHP_N_BULK	AO	Charge pump negative output of DC to DC
38	CHP_P_NEG	AO	Charge pump positive output of high negative DC to DC
39	CHP_N_NEG	AO	Charge pump negative output of high negative DC to DC
42	XHPL	AO	Headphone driver output L CH
41	XHPR	AO	Headphone driver output R CH
S/PDIF I/O			
7	XSPDIFI	DI	S/PDIF receiver
GPIO			
3	XGPIO_0	DIOL	1). General purpose input/output 0 (default input) 2). LED module 1 output 3). R8051 SPI master clock output Internal pull low, 4mA driving current
4	XGPIO_1	DIOL	1). General purpose input/output 1 (default input) 2). LED module 2 output 3). R8051 SPI master data output Internal pull low, 4mA driving current
8	XGPIO_12	DIOL	1). General purpose input/output 12 (default input) 2). LED module 1 output 3). I2S DAC5 master clock output
9	XGPIO_13	DIOL	1). General purpose input/output 13 (default input) 2). LED module 2 output 3). I2S DAC5 bit clock input/output
10	XGPIO_14	DIOL	1). General purpose input/output 14 (default input) 2). LED module 3 output 3). I2S DAC5 left/right clock input/output
11	XGPIO_15	DIOL	1). General purpose input/output 15 (default input) 2). I2S DAC5 serial data output
I2C Master Serial Bus			
44	XMSCL	DIOH	1). I2C master serial clock 2). R8051 I2C serial clock
45	XMSDA	DIOH	1). I2C master serial data 2). R8051 I2C serial data

I2C Slave Serial Bus			
46	XSSCL	DIOH	1). I2C slave serial clock 2). R8051 I2C serial clock (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
47	XSSDA	DIOH	1). I2C slave serial data 2). R8051 I2C serial data (This function is disabled, if R8051 I2C is connected to XMSCL and XMSDA)
Miscellaneous			
12	XSCI	DI	12MHz crystal input
13	XSCO	DO	12MHz crystal output
2	XRSTN	DIH	Reset input, active low
5	XROM	DIL	Reserve for restore to ROM mode
27	NC	-	NC
28	NC	-	NC
32	NC	-	NC
33	NC	-	NC
34	NC	-	NC
35	NC	-	NC
36	NC	-	NC

6 Function Description

6.1 S/PDIF Interface

SPDIF is an audio transmission format in digital domain. The data stream format is illustrated in Fig. 5.1.1. The maximum unit of the S/PDIF stream is a block. A block is composed of 192 frames, and each frame is composed of two subframes. One frame contains one audio sample, so the frame rate is equal to the sampling rate. The left channel audio data is carried by bit slot 4-27 (or time slot 4-27) of subframe A, and right channel is carried by bit slot 4-27 of subframe B. The Sync slot takes preamble signal which is used to label the beginning of a subframe. There are three types for preamble signal, the first is B type, used only in the first subframe of a block; the W type, used in all subframe B; the M format, used in all subframe A, besides the first subframe of a block. The block format is shown in Fig. 7.3.1. The logical level at the start of a bit is always inverted to the level at the end of the previous bit. The level at the end of a bit is equal (a 0 transmitted) or inverted (a 1 transmitted) to the start of that bit.

The S/PDIF data signal is coded by the “biphase-mark-code,” which is a kind of phase modulation. It is illustrated in Fig. 5.1.2. The base clock of a S/PDIF signal is twice the bit rate, and the frequency of the base clock is only determined by the sampling rate. The period of the base clock is called the Unit interval (UI). For example, for a 48KHz 2-channel S/PDIF signal, the frame rate is also 48KHz, so a frame period is 20.833us, and a subframe period is 10.416us. A subframe contains 32-bit slot, so a bit slot period is 325.52ns. As we said above, the base clock is twice the bit rate. Therefore, the period of the base clock is 162.76ns. In other words, the frequency of base clock is 6.144 MHz. Bi-phase coding can prevent PCM data from DC isolated and insensitive to level polarity. A maximum up to 24 data bits can be transmitted by the S/PDIF signal, and the sequence is from LSB to MSB.

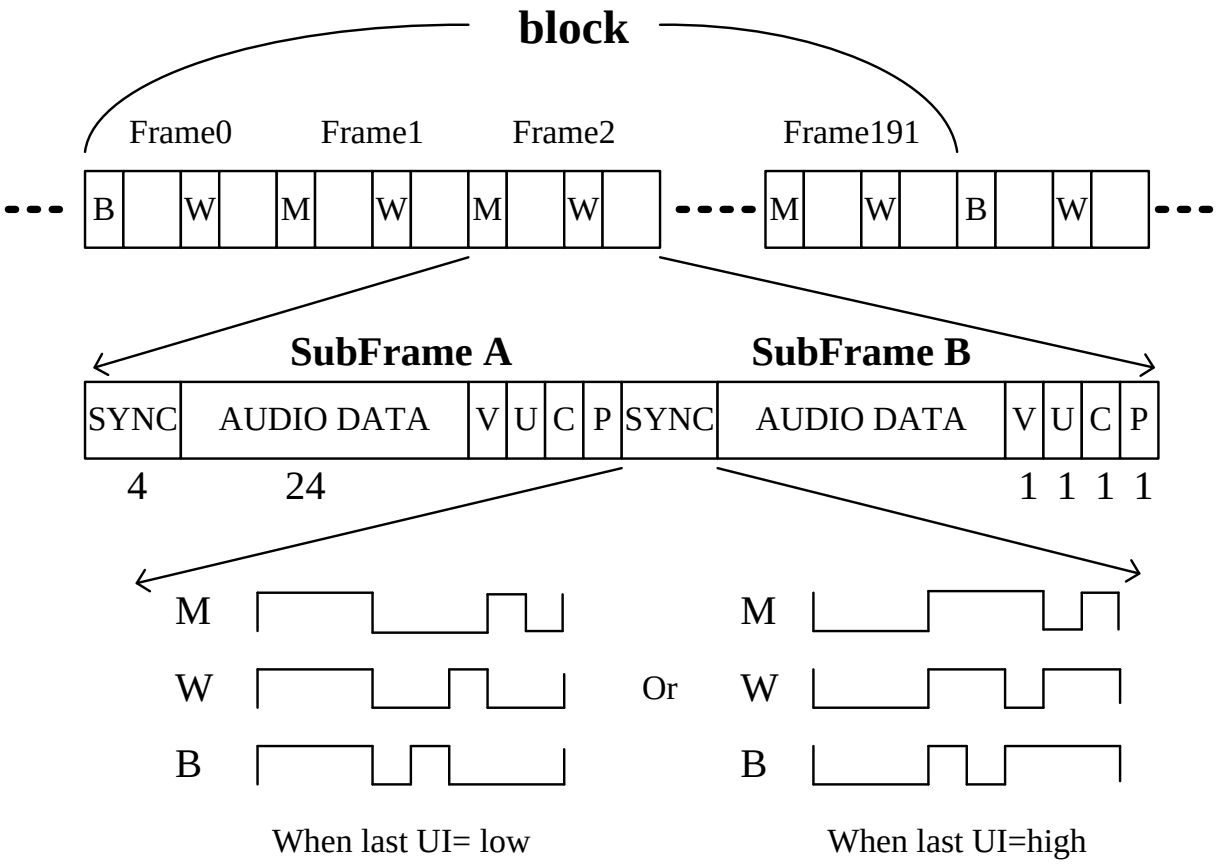


Fig. 5.1.1 S/PDIF Frame format.

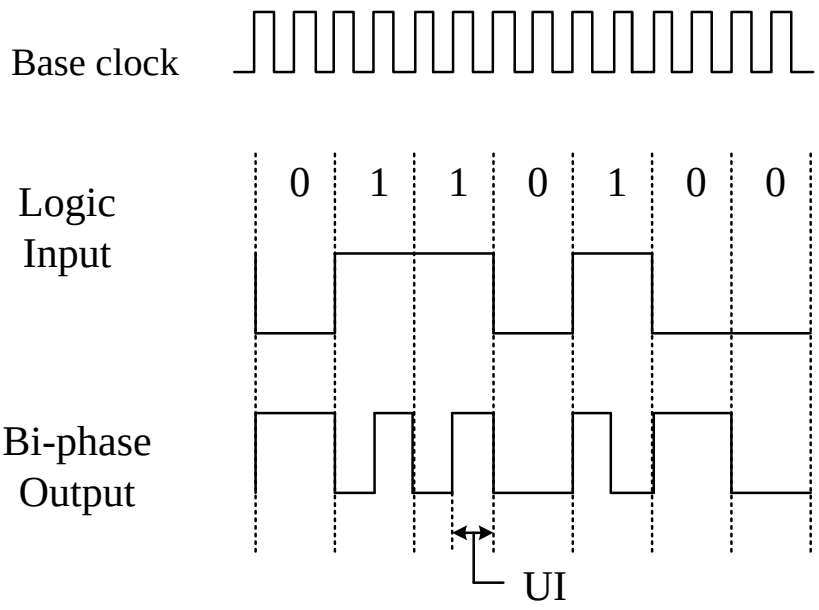


Fig. 5.1.2 S/PDIF biphase-mark-code (BMC).

6.2 Two-Wire Master and Slave Serial Buses (I2C)

The 2-wire master and slave serial buses are designed separately in the CM7037.

6.2.1 The Concept of Two-Wire Bus

The 2-wire bus, as its name reveals, has 2 lines. One is the serial clock line (*SCL*), and the other is the serial data line (*SDA*). Both of them are operated under open drain. That means if the 2 lines are not driven by a master or a slave, they are pulled high by the external pull-up resistors as indicated by Fig. 5.2.1.1. A device connected on the bus can be recognized as a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. Another concept that we should know is the transmitter-receiver relation. *The transmitter is the device which sends data to the bus, and receiver is the device which receives data from the bus.* Note that the definition of transmitter-receiver is different from that of master-slave. We will use these terms to explain 2-wire read/write transactions later. The CM7037 use 7 bits to address the slave devices such as codecs, so theoretically, the 2-wire bus is able to connect 128 slave devices. However, in the audio system application, the limitation is on the codecs, not on the CM7037. Usually, the codecs which support 2-wire bus only have one or two pins to select their address. Therefore, two or four codecs is allowed in the system indicated by Fig. 5.2.1.1, unless the codecs are from different manufactures. In the MCU application, the CM7037 is a slave device, and it can be addressed by the MCU via four different addresses, 0001000b, 0001001b, 0001010b, 0001011b.

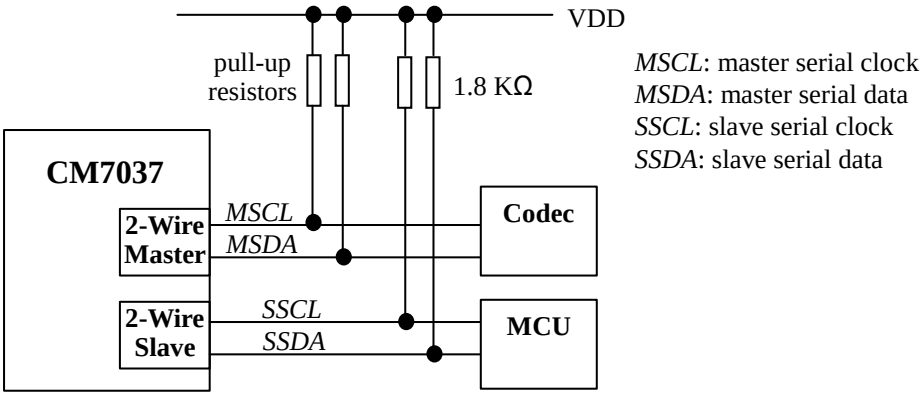


Fig. 5.2.1.1 The connection of 2-wire master and slave buses.

6.2.2 Start and Stop Condition

For a 2-wire bus transaction, the start and stop condition is defined as follows and shown in Fig.5.2.2.1.

- Start: a high to low transition on the *SDA* line while *SCL* is high.
- Stop: a low to high transition on the *SDA* line while *SCL* is high.

Start and stop conditions always generated by the master device. The bus is considered to be busy after the start condition. The bus is considered to be free again after the stop condition.

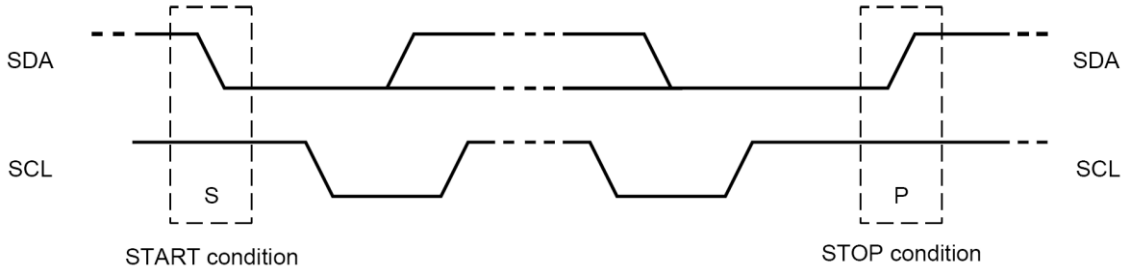


Fig. 5.2.2.1 Start and stop conditions of 2-wire bus.

6.2.3 Bit Transfer

The data on the *SDA* line must be stable during the high period of the clock. The state of the data line can only transit when the clock signal on *SCL* line is low. The bit transfer is indicated in Fig. 5.2.3.1.

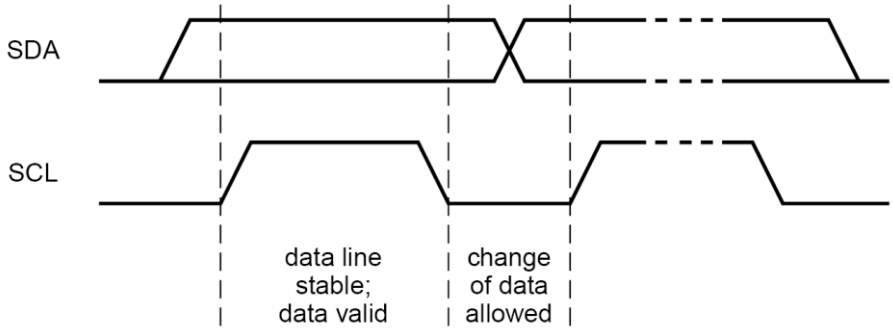


Fig. 5.2.3.1 Bit transfer of 2-wire bus.

6.2.4 Transferring Data with Read/Write Transactions and Acknowledge

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is 3 or 4 bytes in the CM7037. The first byte is always the address byte which is composed of the 7-bit address and 1 read/write bit, listed in Fig. 5.2.4.1 For a write transaction, the second byte is called *Memory Address Pointer* (MAP), which is usually used to indicate the target register in the slave device that the followed third and fourth bytes will be applied on. For a read transaction (only 3 bytes), the second and third bytes is the data returned by the slave device. Each byte has to be ended by an acknowledge bit. Data is transferred with the most significant bit first.

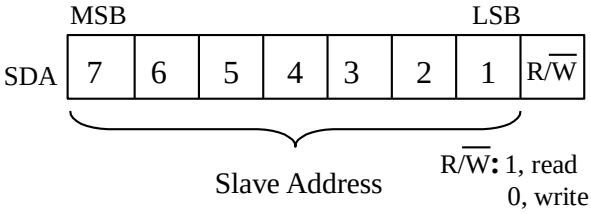


Fig. 5.2.4.1 The first byte after start condition.

The 2-wire master bus of the CM7037 supports read/write transactions. All these transactions are depicted in Fig. 5.2.4.2 to give a whole picture about what the CM7037 can do.

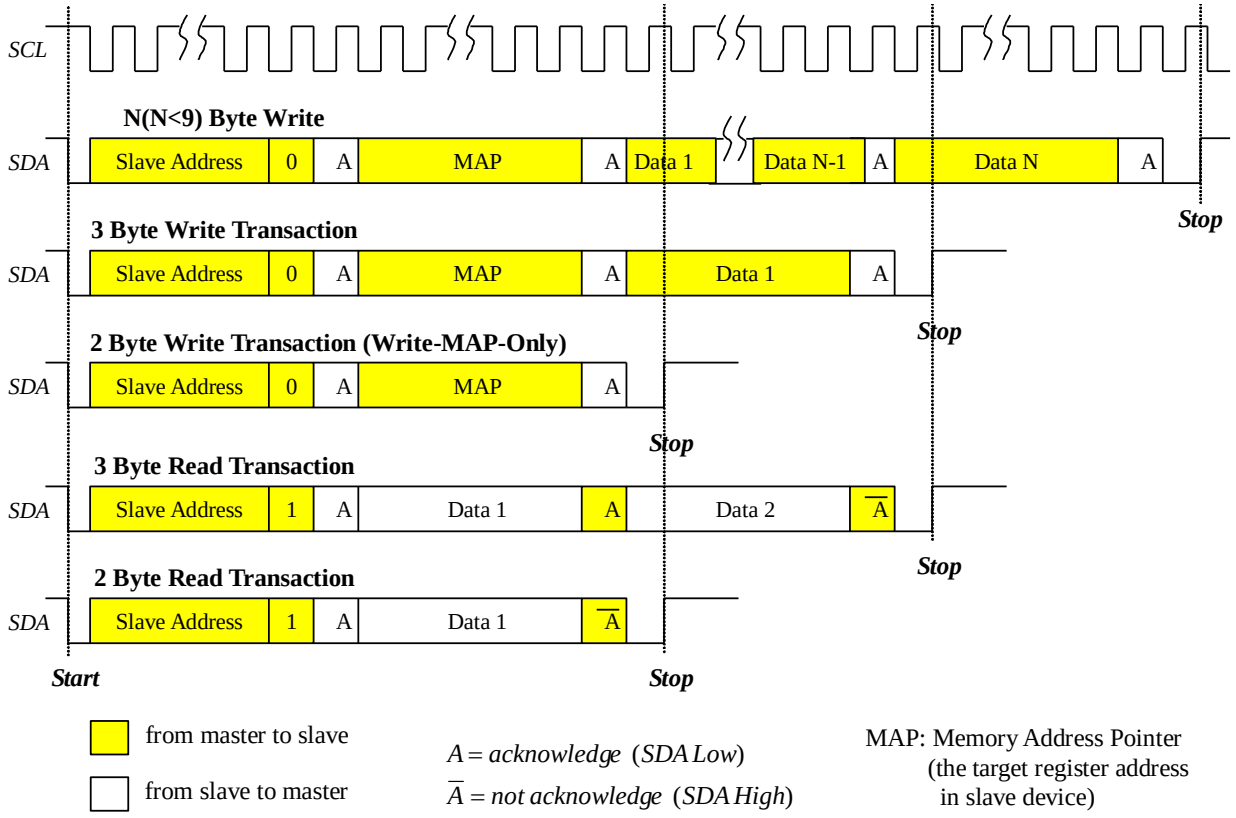


Fig. 5.2.4.2 The 5 basic transactions of the 2-wire master bus supported by the CM7037.

In a read transaction, usually the slave device returns the data of the register whose address is in the MAP. If the read transaction is a 3 byte read transaction, the second returned byte is the data in the (address+1) register. Therefore, the action of obtaining the data in slave device is composed of two transactions, namely a 2 byte write transaction (Write-MAP-Only) followed by a read transaction. For the convenience of users, we have designed an auto read transaction, shown in Fig. 5.2.4.3, which is actually the combination of a write and a read transactions.

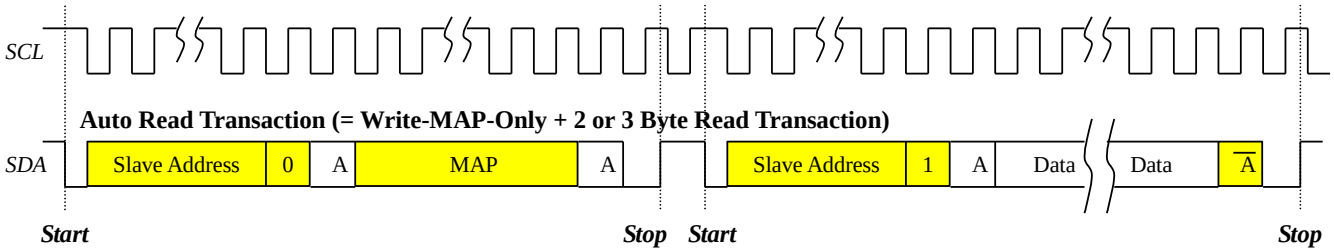


Fig. 5.2.4.3 Auto read transaction in the CM7037.

Data transfer with acknowledge is obligatory. The transmitter release SDA line during the acknowledge clock pulse. Then, the receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low for the entire acknowledge clock high period. This is shown in Fig. 5.2.4.4. When a salve does not acknowledge the slave address byte. For example, it is unable to receive or transmit because it is performing some real-time function. The data line should be left high by the slave. The master can then generate either a stop condition to abort the transfer, or a repeated start condition to start a new transfer.

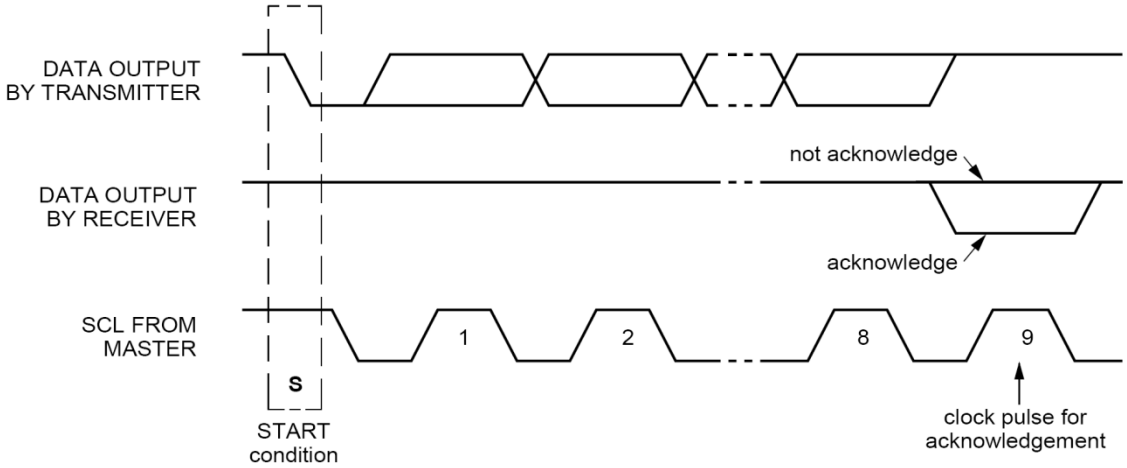


Fig. 5.2.4.4 Acknowledge of the 2-wire bus.

For a read transaction, after the slave address byte is transmitted and acknowledged by slave device, the role of master-transmitter is altered to become master-receiver, and the original slave-receiver is altered to become slave-transmitter. This conception can be easily observed in Fig. 5.2.4.3 and 5.2.4.4, where we use yellow and white blocks to denote the data bit transfer direction. Yellow means the data direction is from the master to the slave. White means the data direction is from the slave to the master. Meanwhile, in a read transaction, the master-receiver must signal the end of the data to the slave transmitter by generating a not-acknowledge ($\overline{A}$) on the last byte that was clocked out of the slave-transmitter. The slave-transmitter should release the *SDA* line to allow the

master to generate a stop or repeated start condition.

6.2.5 Synchronization

The synchronization of the 2-wire bus in the CM7037 can be described in two aspects. The first aspect is the synchronization used in arbitration. Although we did not implement arbitration, we did implement clock synchronization. Clock synchronization is used when there are more than two masters connected on the bus. A high to low transition on the *SCL* line will cause the concerned masters start counting the clock low period. Before the clock high state is reached, the masters will hold the *SCL* line in low state. However, the low to high clock transition of one of the masters may not change the state of the *SCL* line if another master's clock is still in low period (because the *SCL* line of the devices are wire-AND connected by open-drain technique). Therefore, the *SCL* line will be held low by the device with the longest clock low period. The other devices with shorter low period, including the CM7037, enter a high wait state during this time. Figure 5.2.5.1 listed below is the timing of clock synchronization.

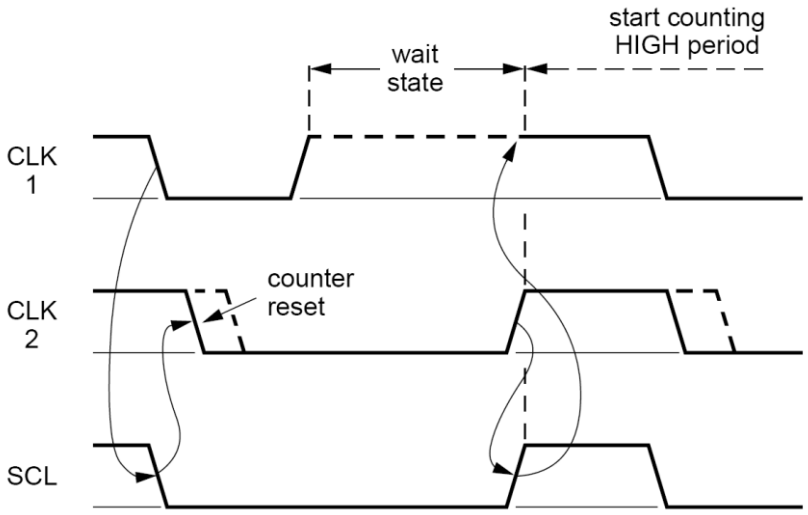


Fig. 5.2.5.1 Clock synchronization for more than two masters in the bus.

Another aspect of synchronization is the data synchronization between master and slave. If a slave cannot receive or transmit another complete byte of the data until it has performed some other function, for example servicing an internal interrupt or waiting for the driver to prepare the data needed, the salve can hold the clock line *SCL* low to force the master into a wait state. Data transfer then continues when the slave is ready and releases the clock line *SCL*. The data synchronization is shown in Fig. 5.2.5.2.

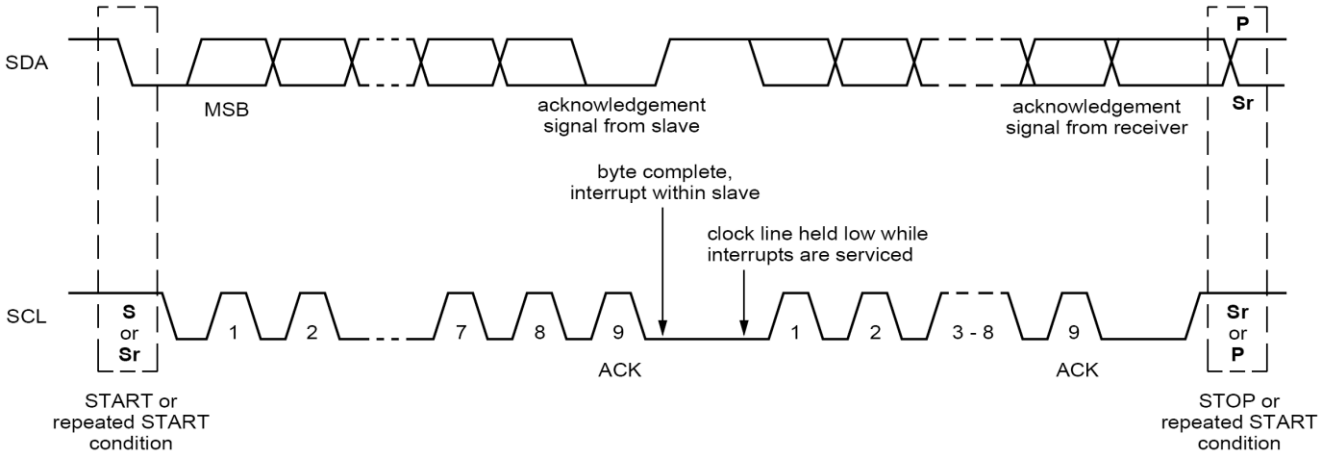


Fig. 5.2.5.2 The data synchronization of the 2-wire master and slave buses in the CM7037.

6.2.6 Standard Mode and Fast Mode

Both the 2-wire master and slave buses in the CM7037 can support standard mode transfer and fast mode transfer. The data transfer rate of the standard mode is up to 100 Kbits/sec, and the fast mode is up to 400 Kbits/sec. The clock timing of these modes are listed in Fig. 5.2.6.1 and Table 5.2.6.1

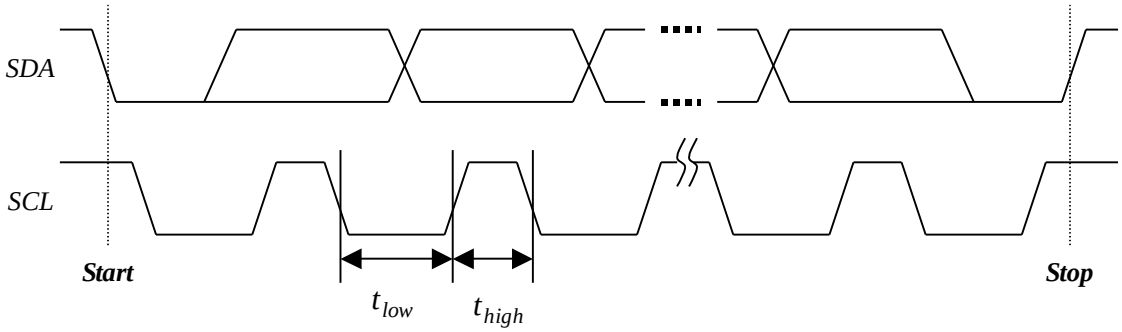


Fig. 5.2.6.1 Standard mode and fast mode timing.

Table 5.2.6.1 Standard mode and fast mode timing.

Parameter	Symbol	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Low period of *SCL* clock	t_{low}	4.8	—	1.3	—	μS
High period of *SCL* clock	t_{high}	4.8	—	0.6	—	μS

6.3 GPIO

All the GPIO pins can be configured as input or output by the GPIO direction control registers and also can be configure as remote wake up input pin. If they are assigned as outputs, then the contents in the GPIO data registers will be reflected to the corresponding GPIO pins. If they are assigned as inputs, they can be used for jack activity detection. If a speaker is plugged or unplugged, the state of the pin connected with that jack will be changed. As a result, an interrupt is issued to R8051, and an interrupt mask control bit is utilized to decide if the interrupt from that corresponding GPIO pin should be sent. After receiving the interrupt, R8051 must read the GPIO data register (address offset 0x0300h) to discover what pins have changed their states. Then, the R8051 will make some appropriate manipulation in response to the jack activity.

CM7037 supports two kinds of Remote-wakeup. One is hardware Remote-wakeup, and the other is software Remote-wakeup. When in Configuration, CM7037 has to report the host via the descriptor whether CM7037 supports the Remote-wakeup or not. If CM7037 reports it supports Remote-wakeup and the host also supports Remote-wakeup, the host will issue the request of Set-feature to enable the Remote-Wakeup feature. If the user selects hardware Remote-wakeup, the user has to select one of the GPIOs to configure as a remote wakeup pin. If there is a transition from 0 to 1 on this pin, that will cause a remote-wakeup to wake up the host from the suspend state. The transition can be from outer world or from the control of the R8051. If the transition is from the control of the R8051, this is called Software Remote-wakeup. Software Remote-wakeup is implemented by the register. If the user selects software Remote-wakeup, the 8051 has to write the register to cause the transition from 0 to 1 to wake up the host.

CM7037 has a de-bouncing circuit to filter the interrupt to R8051. There are two options to select which are 16ms and 8ms. The user can select one option to use according to their application.

6.4 I2S Interface

The digital audio interface of the CM7037 is I^2S, which has three clock signals, MCLK, BCLK and LRCK, and at least one data line depending on the channels supported. One data line contains two channels. The three I^2S clock symbols are explained below.

MCLK = main clock.
BCLK = bit clock.
LRCK = left and right clock.

6.4.1 The Basics of I2S Bus

CM7037 can support I2S output master mode only. Master mode means BCLK and LRCK are provided by the CM7037 as shown in Fig. 5.4.1 (a).

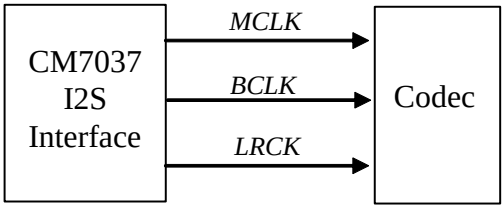


Fig. 5.4.1 (a) Master mode;

Fig. 5.4.1 (b) indicates the basic waveform of I2S. Note that BCLK is generated at the positive edges of MCLK with the ratios 1, 1/2, 1/4, or 1/8, and LRCK is generated at the negative edges of BCLK with the ratios 1/64, 1/128, 1/256. Data bits are transited at the negative edges of BCLK, and are sampled at the positive edges of BCLK. In case of playback, CM7037 is the data transmitter and the codec is the data receiver. As for recording, the roles of CM7037 and codec are reversed.

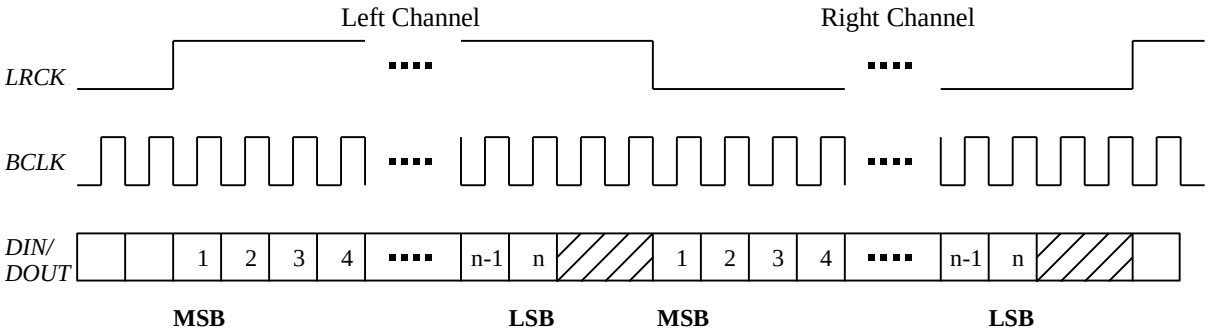


Fig. 5.4.1 (b) The basic timing diagram of the I2S interface.

For the I2S output controller, the audio data is transformed from the parallel format to the serial format before transmitted. Then, the bit data is shifted out one by one with the MSB first via DOUT signal. If the I2S DAC controller is set to 32 bits, at least 32 BCLK clocks must exist in both LRCK left and right channels.

6.4.2 Left Justified Mode

In the left justified mode of the I2S output controller, the MSB data bit is clocked out by the CM7037 at the negative edge of BCLK which is aligned to the transition of LRCK. LRCK is high during left channel transmission and low during right channel transmission in the left justified mode. Fig. 5.4.2 shows all of these.

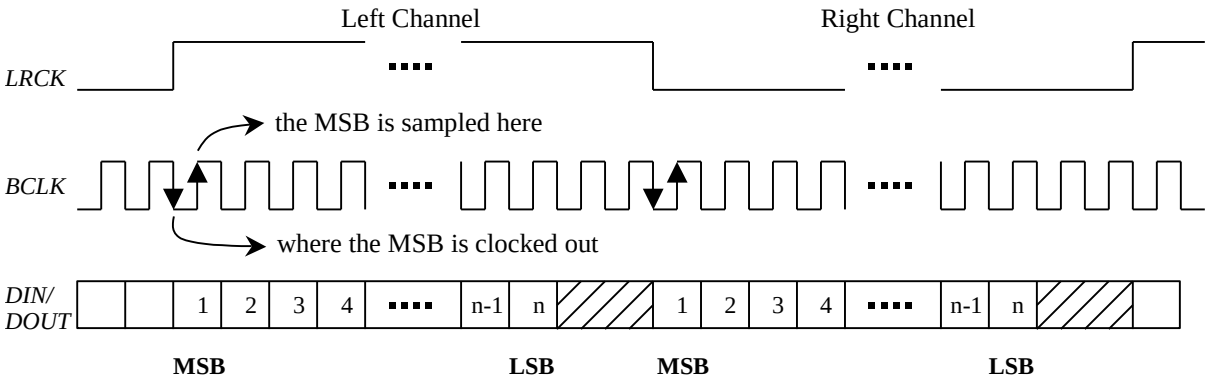


Fig. 5.4.2 Left justified mode timing diagram of I2S interface.

6.4.3 I2S Mode

In the I2S mode of the I2S output controller, the MSB data bit is clocked out by CM7037 at the first negative edge of BCLK which follows a LRCK transition. LRCK is low during left channel transmission and high during right channel transmission in the I2S mode. Fig. 5.4.3 indicates all of these.

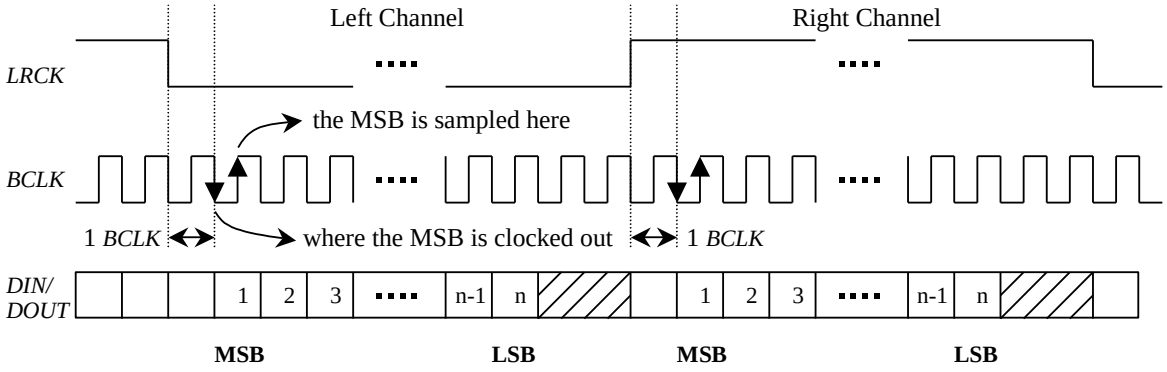


Fig. 5.4.3 I2S mode timing diagram of I2S interface.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-40	-	125	°C
Digital supply voltage	XD5V_XA5V	-	-	5.5	V
ESD (Body mode)	HBM	-	±4000	-	V
ESD (Machine mode)	MM	-	±200	-	V

7.2 Recommended Operation Conditions

Parameter	Symbol	Min.	Typ	Max.	Units
Operating ambient temperature	T_A	0	25	70	°C
Supply voltage	XD5V_XA5V	4.085	4.3	4.515	V
Digital Core	VCC12	1.08	1.2	1.32	V

7.3 Power Consumption

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, TA=+25°C, MCU Clock = 6MHz.
Sample Rate=48kHz, 24Bits, Operation: Headphone output and SPDIF input,
Volume setting = Gain 0dB

Parameter	Symbol	Min.	Typ	Max.	Units
Total power consumption (Playback + Record)	-	-	54	-	mA
Standby power consumption	-	-	51	-	mA
Suspend mode power consumption	-	-	1.1	-	mA

7.4 DC Characteristics

Test Conditions: XD5V_XA5V = 4.3V, AGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Units
Input voltage range	DI	0	-	3.6	V
Output voltage rage	DO	0	-	3.6	V
High-level input voltage	Vih	2.0	-	-	V
Low-level input voltage	Vil	-	-	0.8	V
High-level output voltage	Voh	2.4	-	-	V
Low-level output voltage	Vol	-	-	0.4	V

8 Analog Performance

8.1 DAC audio quality (Phone Jack)

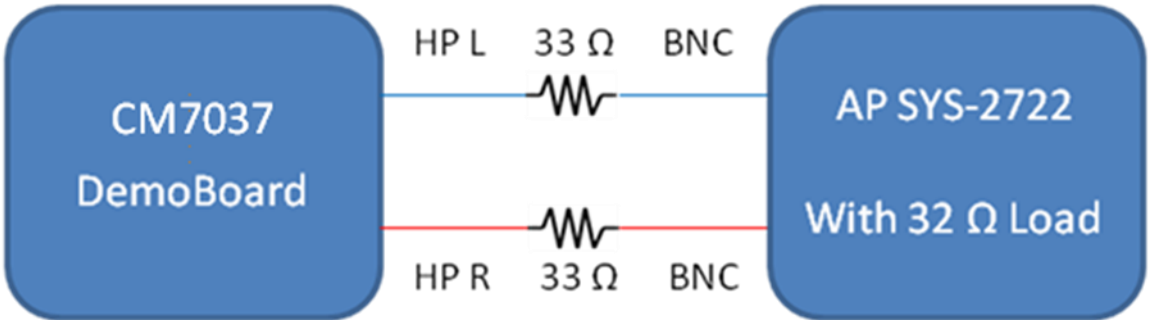
TA=25℃, XD5V_XA5V = 4.3V, AGND =0V, Equalizer disable,
Platform:HP EliteBook 840r G4 8G RAM, Windows 10 CHT
Test AP: SYS-2722
Player：Foobar2000

Items	Test Conditions			Test Values			Unit
				Min.	Typ.(1KHZ)	Max.	
Full Scale Output Voltage	10KΩ loading				1043		mVrms
	32Ω loading				900		
	32Ω loading with 33 ohm cascade				477		
THD+N With None Filter.	10KΩ Loading	0dBFS (Fig1)	44.1K/16bits		-89.0		dB
			48K/16bits		-90.1		
			96K/24bits		-90.4		
			192K/24bits		-87.7		
		-3dBFS (Fig2)	44.1K/16bits		-89.6		dB
			48K/16bits		-90.4		
			96K/24bits		-91.2		
			192K/24bits		-91.8		
	32Ω Loading	0dBFS (Fig3)	44.1K/16bits		-79.4		dB
			48K/16bits		-79.3		
			96K/24bits		-79.6		
			192K/24bits		-79.5		
		-3dBFS (Fig4)	44.1K/16bits		-81.0		dB
			48K/16bits		-81.1		
			96K/24bits		-81.6		
			192K/24bits		-82.3		
	32Ω loading Cascade 33 ohm	0dBFS (Fig5)	44.1K/16bits		-81.7		dB
			48K/16bits		-81.7		
			96K/24bits		-83.4		
			192K/24bits		-83.2		
		-3dBFS (Fig6)	44.1K/16bits		-85.0		dB
			48K/16bits		-85.5		
			96K/24bits		-86.1		
			192K/24bits		-84.9		

Items	Test Conditions		Test Values			Unit
			Min.	Typ.(1KHZ)	Max.	
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave	10KΩ loading	44.1K/16bits		-93.6		dB
		48K/16bits		-94.9		
		96K/24bits		-94.4		
		192K/24bits		-95.3		
	32Ω loading	44.1K/16bits		-93.6		dB
		48K/16bits		-94.6		
		96K/24bits		-95.1		
		192K/24bits		-95.6		
	32Ω loading Cascade 33 ohm	44.1K/16bits		-93.5		dB
		48K/16bits		-94.6		
		96K/24bits		-94.4		
		192K/24bits		-94.6		
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave	10KΩ loading	44.1K/16bits		-94.8		dB
		48K/16bits		-95.3		
		96K/24bits		-95.8		
		192K/24bits		-95.3		
	32Ω loading	44.1K/16bits		-95.1		dB
		48K/16bits		-96.2		
		96K/24bits		-95.6		
		192K/24bits		-95.6		
	32Ω loading Cascade 33 ohm	44.1K/16bits		-94.6		dB
		48K/16bits		-95.4		
		96K/24bits		-95.4		
		192K/24bits		-95.4		
			100		10K	HZ
Channel Separation (Cross-talk)	10KΩ Loading (Fig7)	44.1K/16bits	-108.8		-101.8	dB
		48K/16bits	-112.3		-101.8	
		96K/24bits	-110.1		-102.5	
		192K/24bits	-110.4		-102.5	
	32Ω Loading (Fig8)	44.1K/16bits	-93.7		-75.1	dB
		48K/16bits	-94.0		-75.4	
		96K/24bits	-93.9		-75.4	
		192K/24bits	-93.7		-75.2	
	32Ω loading Cascade 33 ohm(Fig9)	44.1K/16bits	-101.7		-80.5	dB
		48K/16bits	-102.9		-80.4	
		96K/24bits	-101.1		-80.2	
		192K/24bits	-102.5		-80.3	

Items	Test Conditions		Test Values			Unit
				Typ.(1KHZ)		
	Band Edge		20	-	20K	HZ
Frequency Response	10KΩ Loading (Fig10)	44.1K/16bits	0.1		-4.6	dB
		48K/16bits	0.1		-1.0	
		96K/24bits	0.1		-0.3	
		192K/24bits	0.04		-0.2	
	32Ω Loading (Fig11)	44.1K/16bits	0.1		-4.6	dB
		48K/16bits	0.1		-1.0	
		96K/24bits	0.02		-0.3	
		192K/24bits	0.02		-0.2	
	32Ω loading Cascade 33 ohm (Fig12)	44.1K/16bits	0.1		-4.6	dB
		48K/16bits	0.1		-1.0	
		96K/24bits	0.1		-0.4	
		192K/24bits	0.05		-0.3	
Passband Ripple	10KΩ loading	44.1K/16bits		0.29		dB
		48K/16bits		0.28		
		96K/24bits		0.32		
		192K/24bits		0.30		
	32Ω loading	44.1K/16bits		0.24		dB
		48K/16bits		0.23		
		96K/24bits		0.27		
		192K/24bits		0.21		
	32Ω loading Cascade 33 ohm	44.1K/16bits		0.33		dB
		48K/16bits		0.27		
		96K/24bits		0.22		
		192K/24bits		0.22		
Interchannel phase delay	10KΩ Loading (Fig13)	44.1K/16bits		0.05		%
		48K/16bits		0.04		
		96K/24bits		0.02		
		192K/24bits		0.02		
	32Ω Loading (Fig14)	44.1K/16bits		0.01		%
		48K/16bits		-0.01		
		96K/24bits		-0.04		
		192K/24bits		0.01		
	32Ω loading Cascade 33 ohm (Fig15)	44.1K/16bits		0.04		%
		48K/16bits		0.05		
		96K/24bits		-0.04		
		192K/24bits		-0.04		

Note: Headphone 32 ohm loading audio quality measure by cascading 33 or 0 ohm resistors, the schematic diagram as below.



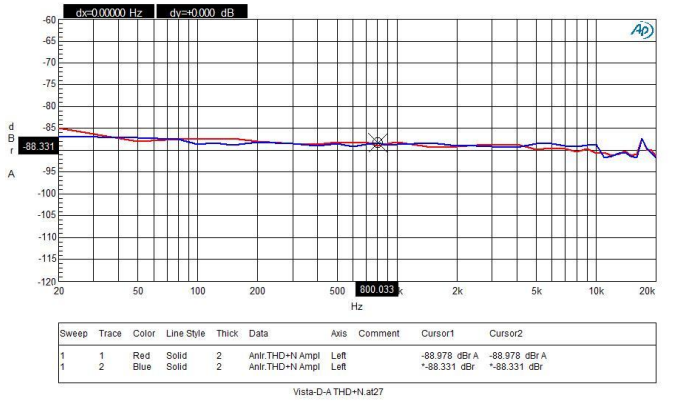
8.2 I2S Out audio quality

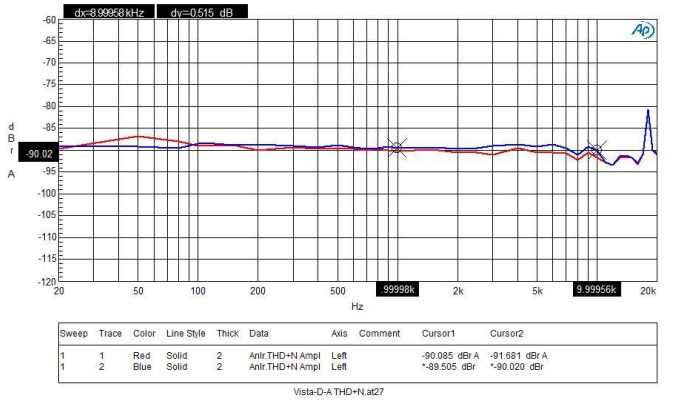
TA=25℃, XD5V_XA5V = 4.3V, AGND =0V, Equalizer disable,
Platform:HP EliteBook 840r G4 8G RAM, Windows 10 CHT
Test AP: AP-525 I2S Analyzer
Player：AP525 Generator_Digital Optical

Items	Test Conditions		Test Values			Unit
			Min.	Typ.(1KHZ)	Max.	
THD+N With None Filter.	0dBFS	44.1K/16bits	--	-93.5	--	dB
		48K/16bits	--	-93.5	--	
		96K/24bits	--	-141	--	
		192K/24bits	--	-141	--	
	-3dBFS	44.1K/16bits	--	-90.5	--	dB
		48K/16bits	--	-90.5	--	
		96K/24bits	--	-141	--	
		192K/24bits	--	-141	--	
Dynamic Range With A-Weighted, test by -60dBFS 1K sine wave		44.1K/16bits	--	-95.8	--	dB
		48K/16bits	--	-96	--	
		96K/24bits	--	-147	--	
		192K/24bits	--	-147	--	
SNR (Noise level during active) With A-Weighted, test by -96dBFS 1K sine wave		44.1K/16bits	--	-95.8	--	dB
		48K/16bits	--	-96	--	
		96K/24bits	--	-147	--	
		192K/24bits	--	-147	--	
Channel Separation (Cross-talk)	Sampling frequency		100	-	10K	HZ
		44.1K/16bits	-93	-	-93	dB
		48K/16bits	-93	-	-93	
		96K/24bits	-141	-	-141	
		192K/24bits	-141	-	-141	
Frequency Response	Band Edge		20	-	20K	HZ
		44.1K/16bits	-0.0035	-	-0.0005	dB
		48K/16bits	-0.0035	-	-0.0005	
		96K/24bits	-0.0035	-	-0.0005	
		192K/24bits	-0.0035	-	-0.0005	
				Typ.(1KHZ)		Unit
Passband Ripple		44.1K/16bits	--	-0.001	--	dB
		48K/16bits	--	-0.001	--	
		96K/24bits	--	-0.001	--	
		192K/24bits	--	-0.001	--	
Interchannel phase delay		44.1K/16bits	--	0	--	degree
		48K/16bits	--	0	--	
		96K/24bits	--	0	--	
		192K/24bits	--	0	--	

Figure 1： DAC 10KΩ loading, 0dB, THD+N

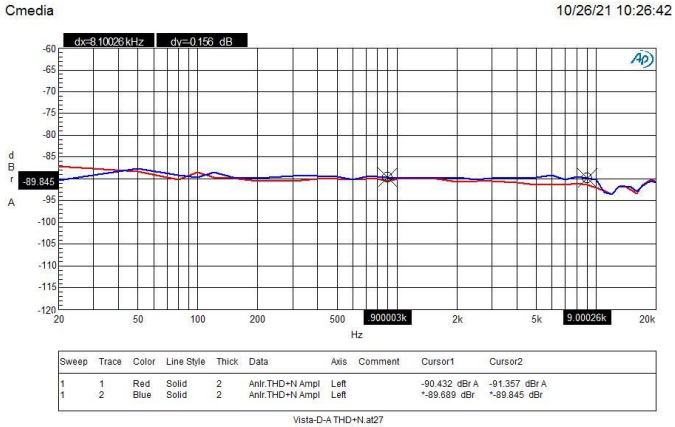
44.1K/16bits	48K/16bits





96K/24bits

192K/24bits



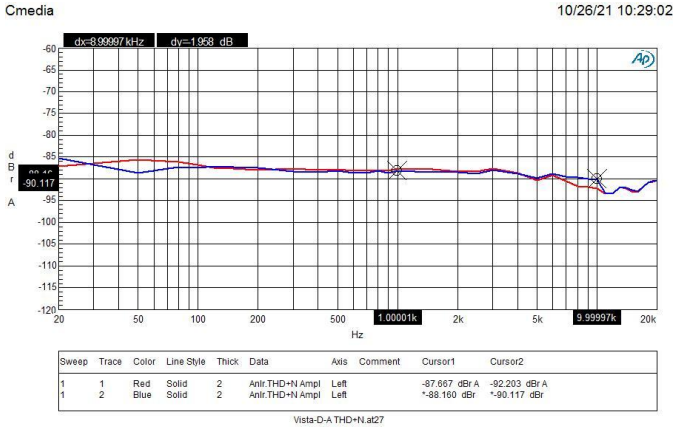


Figure 2： DAC 10KΩ loading, -3dB, THD+N

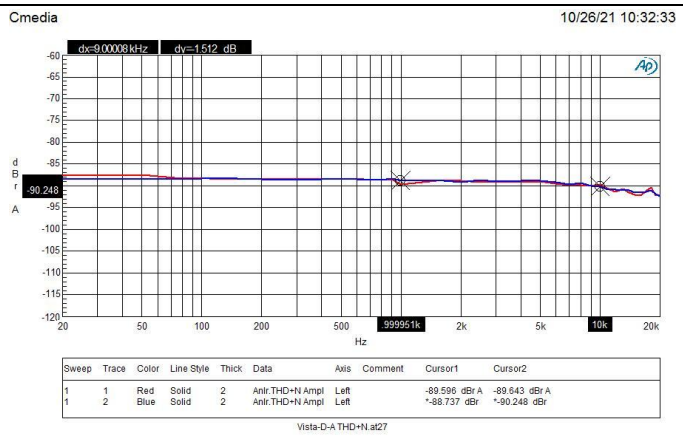
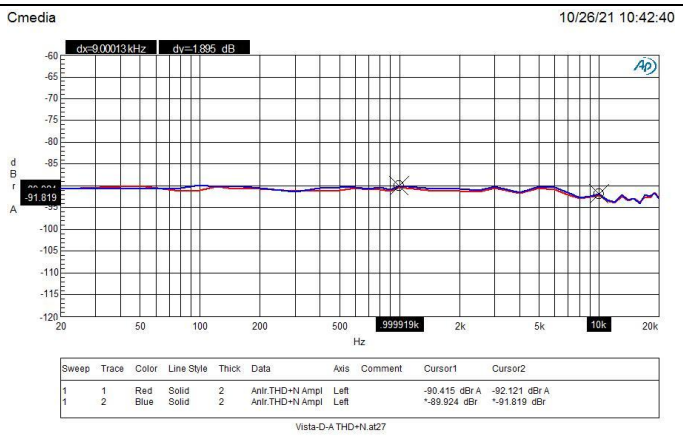
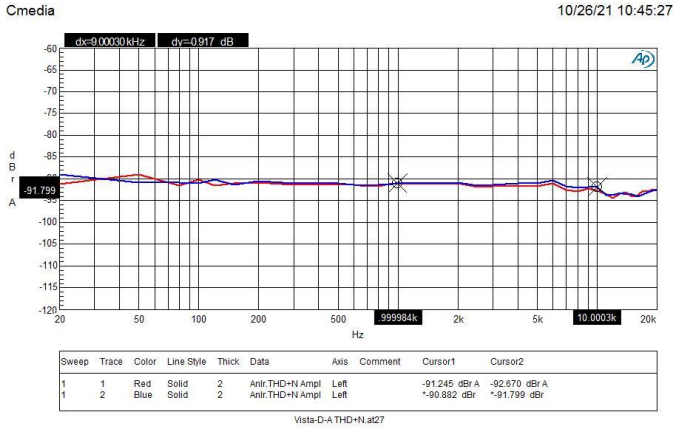
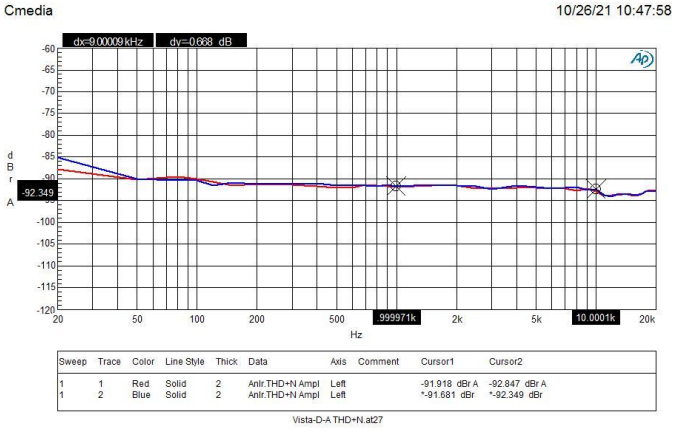
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 3： DAC 32Ω loading, 0dB, THD+N

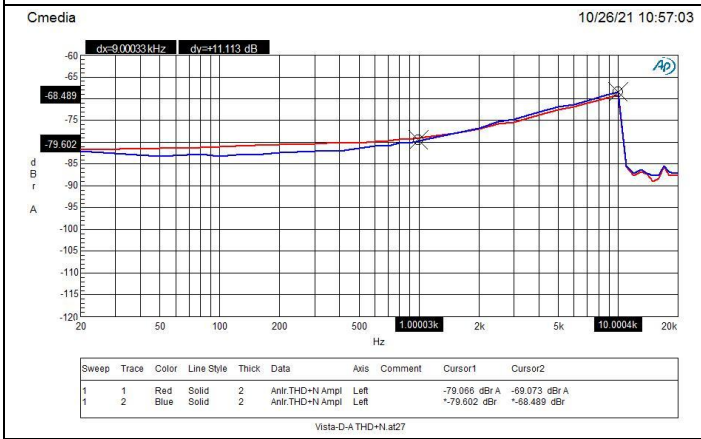
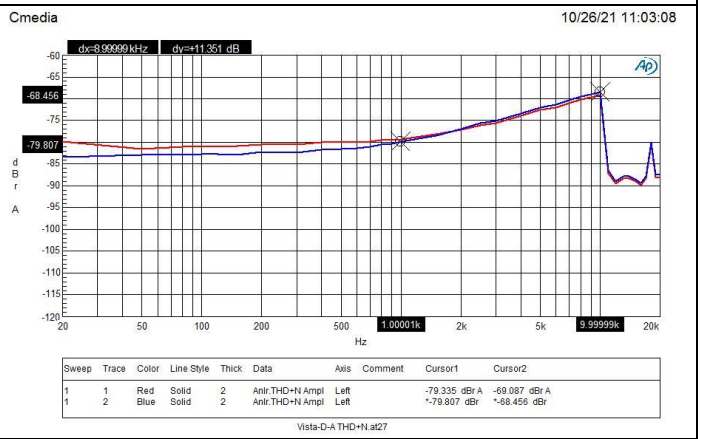
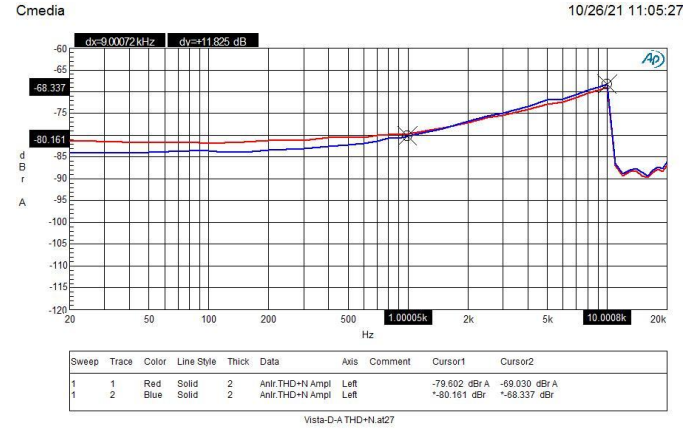
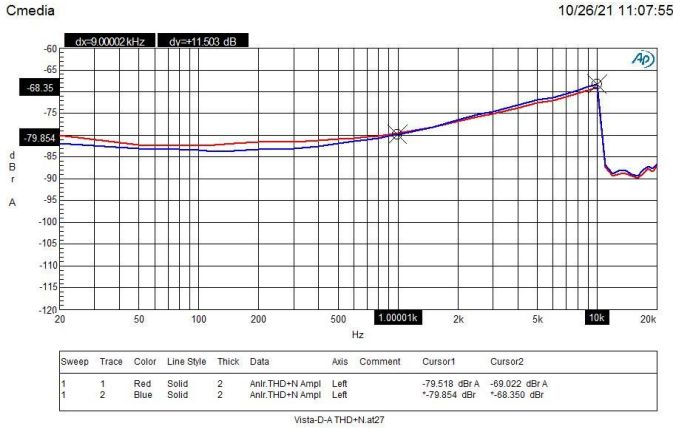
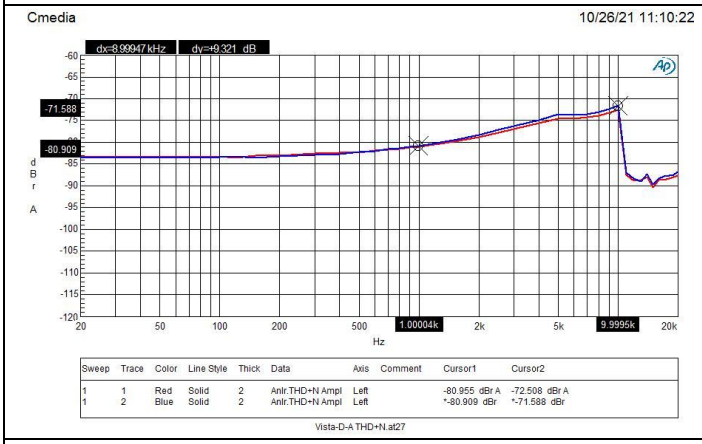
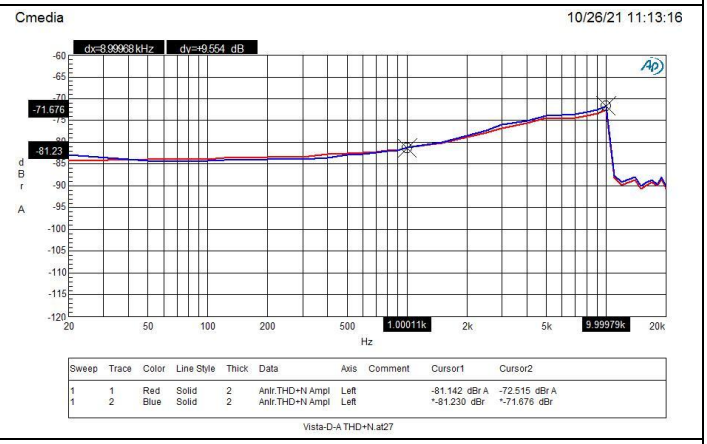
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 4： DAC 32Ω loading, -3dB, THD+N

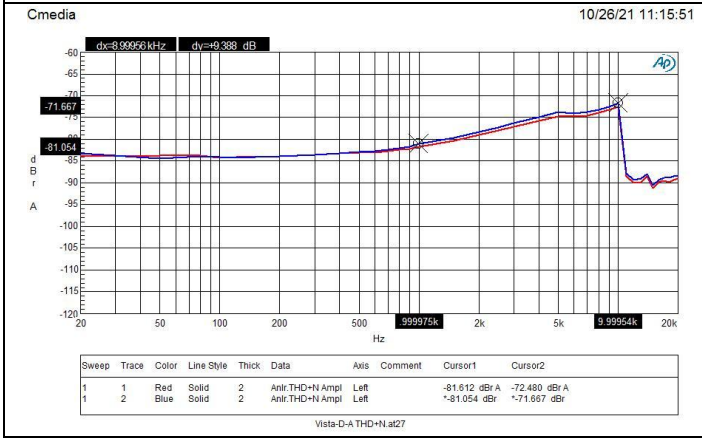
44.1K/16bits



48K/16bits



96K/24bits



192K/24bits

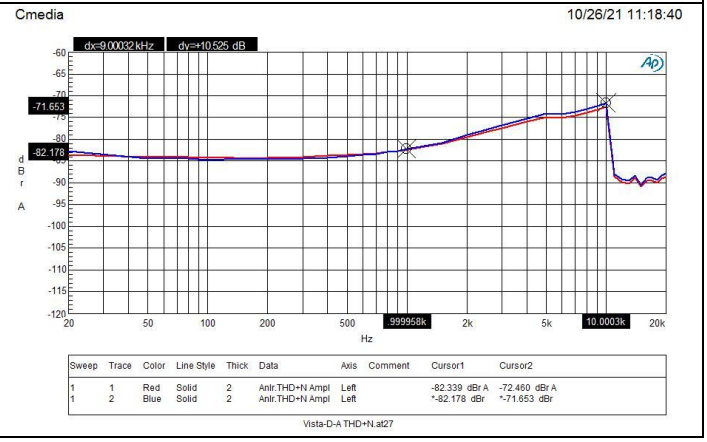


Figure 5： DAC 32Ω loading Cascade 33 ohm, 0dB, THD+N

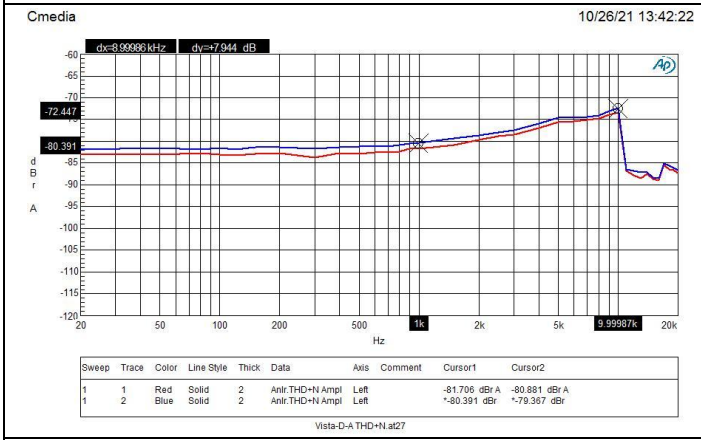
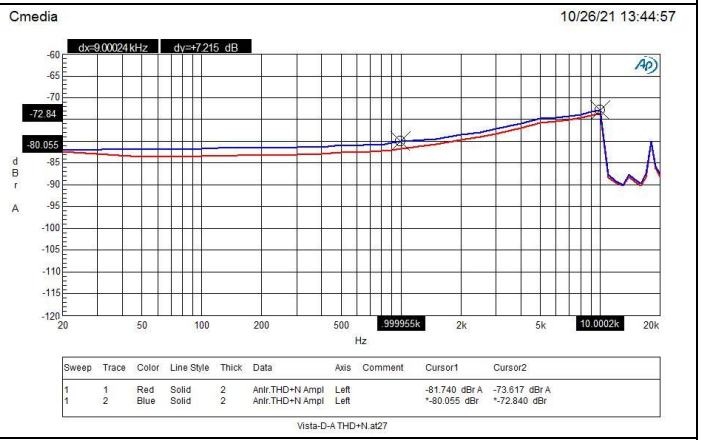
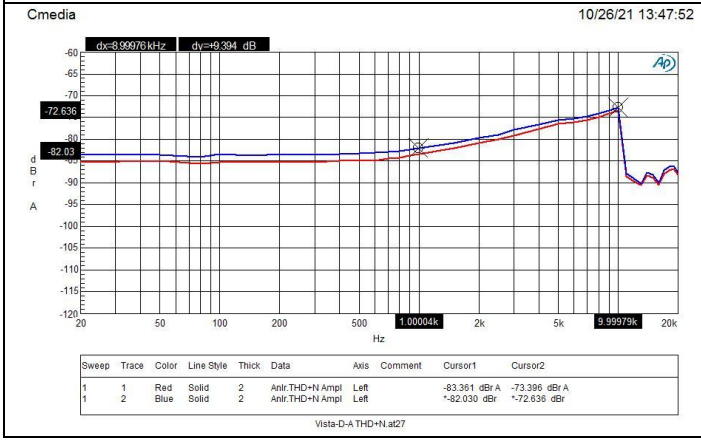
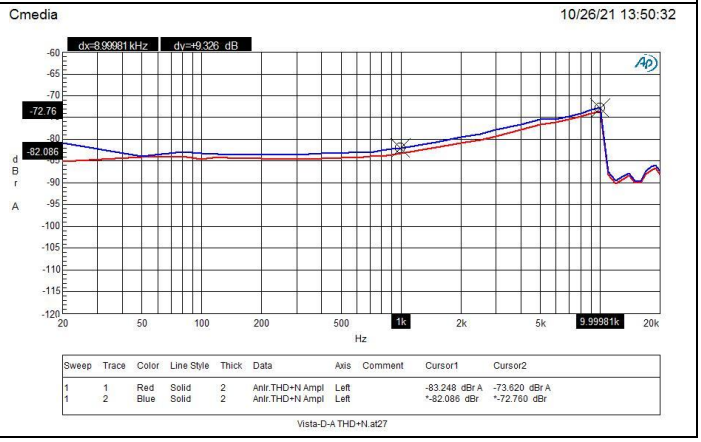
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 6： DAC 32Ω loading Cascade 33 Ω, -3dB, THD+N

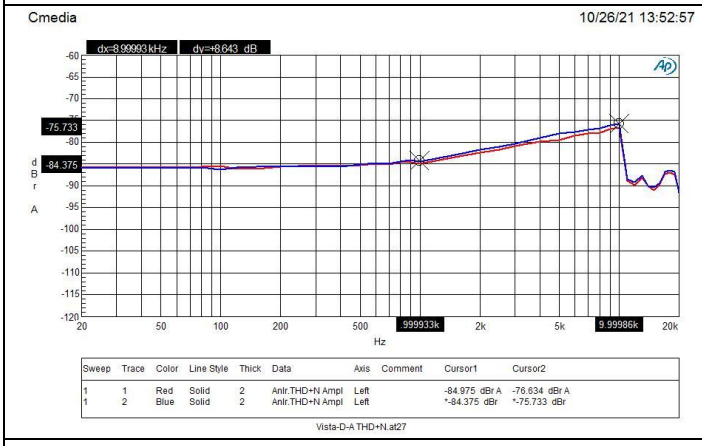
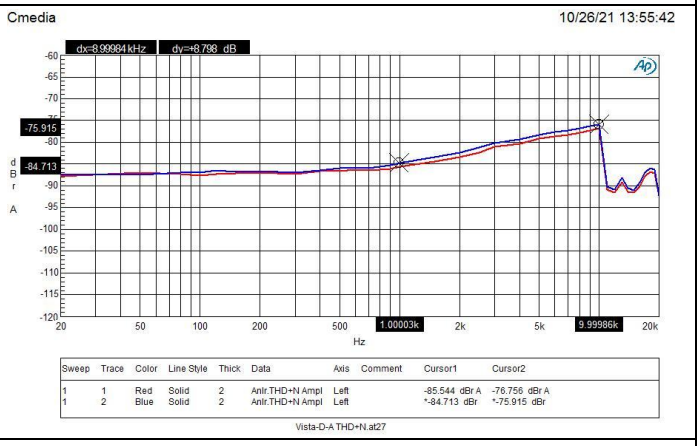
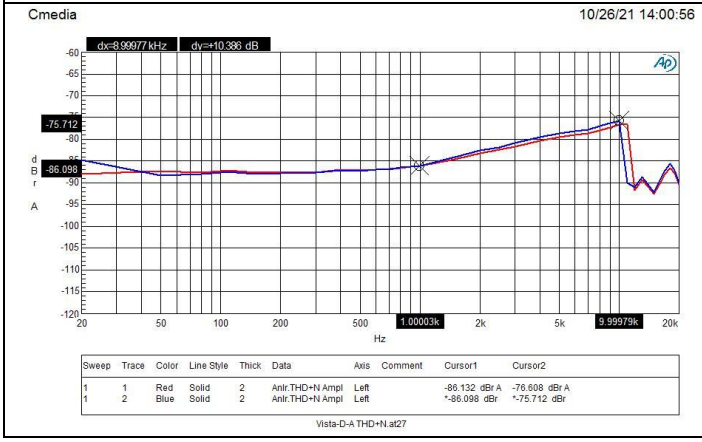
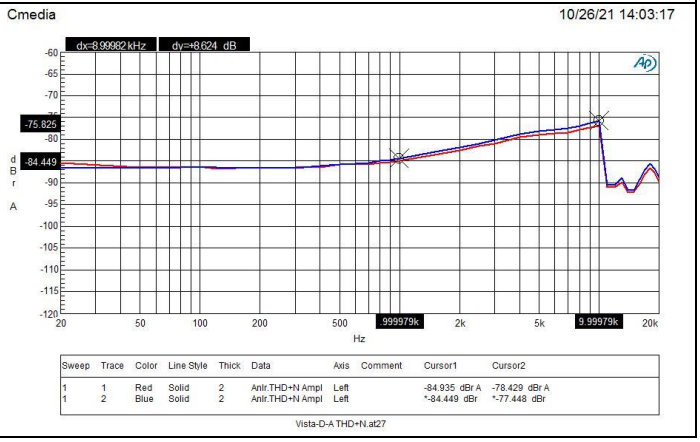
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 7： DAC 10KΩ loading, Cross-talk

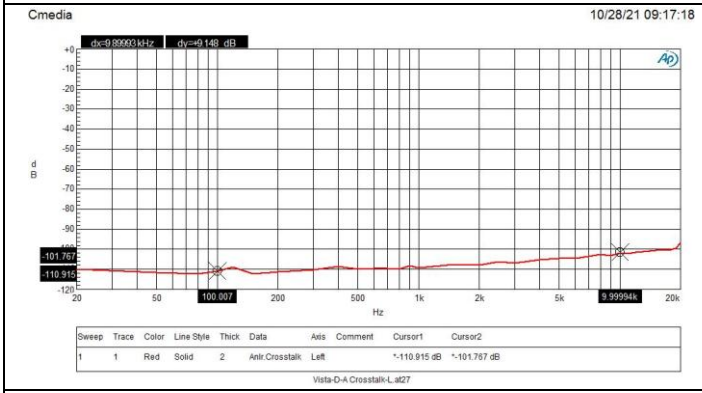
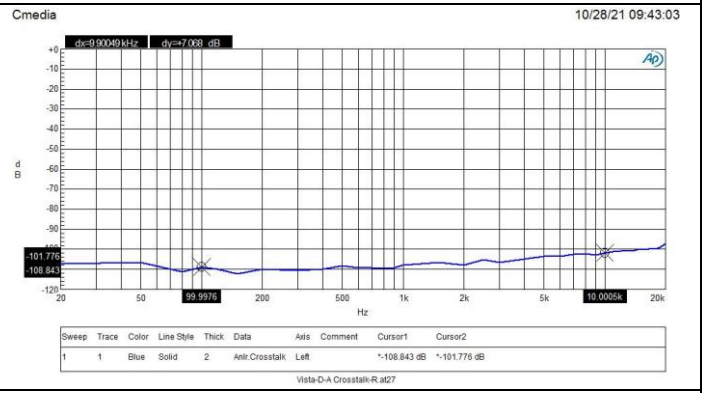
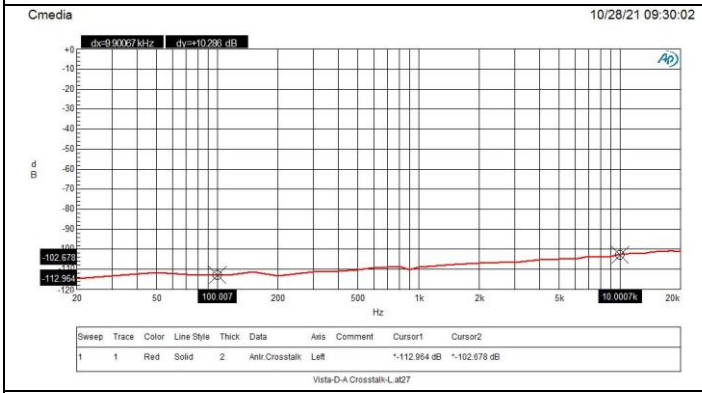
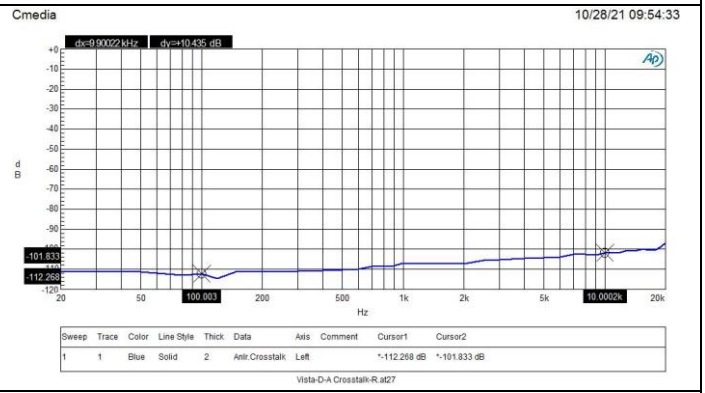
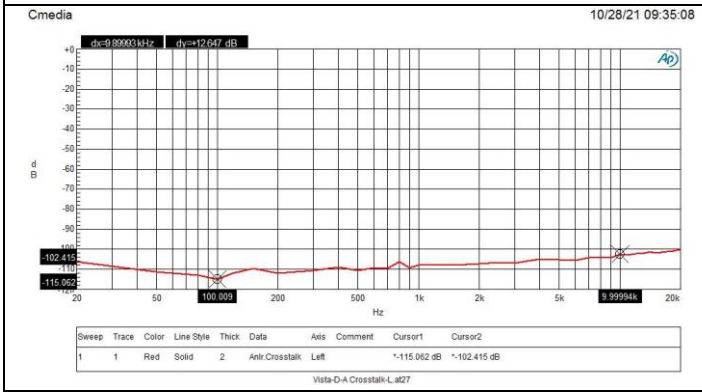
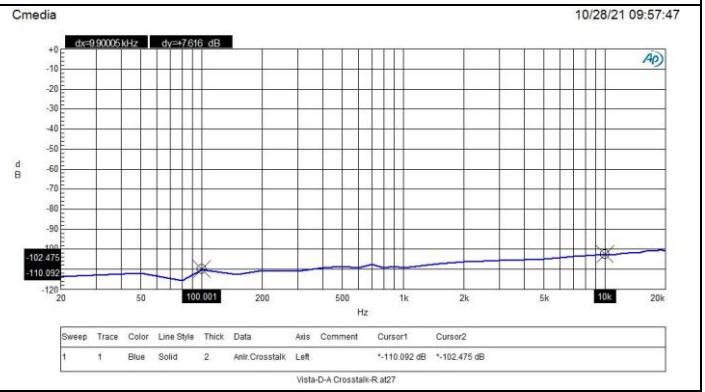
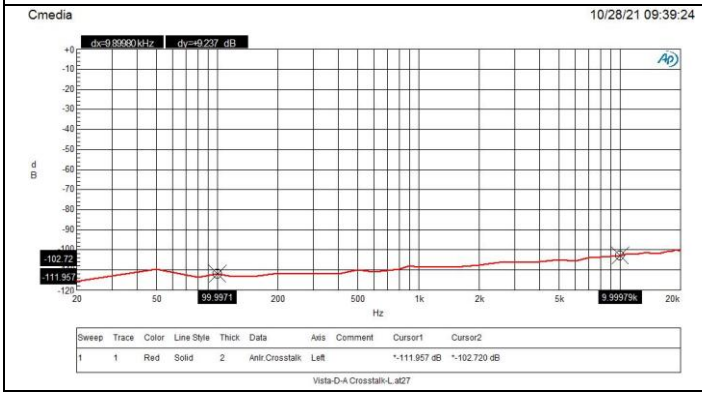
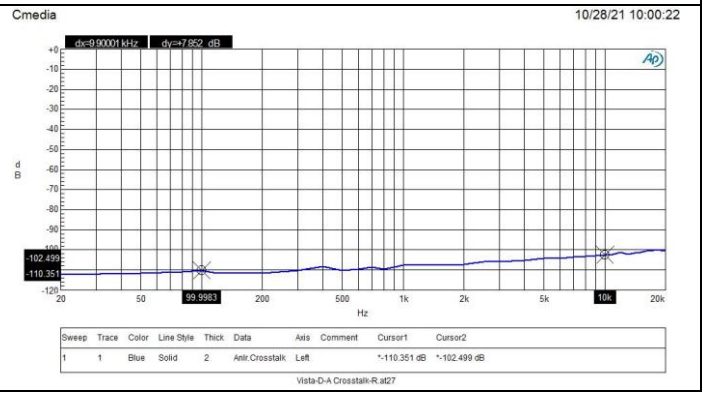
44.1K/16bits L	44.1K/16bits R
	
48K/16bits L	48K/16bits R
	
96K/24bits L	96K/24bits R
	
192K/24bits L	192K/24bits R
	

Figure 8： DAC 32Ω loading, Cross-talk

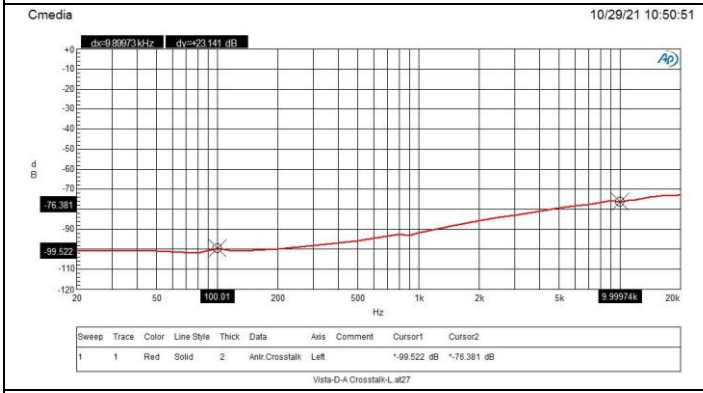
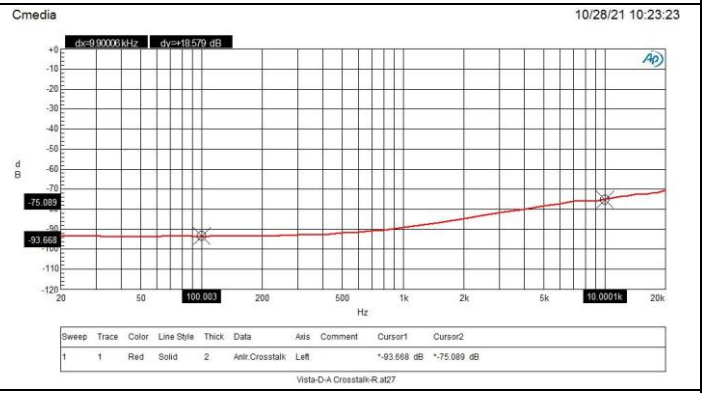
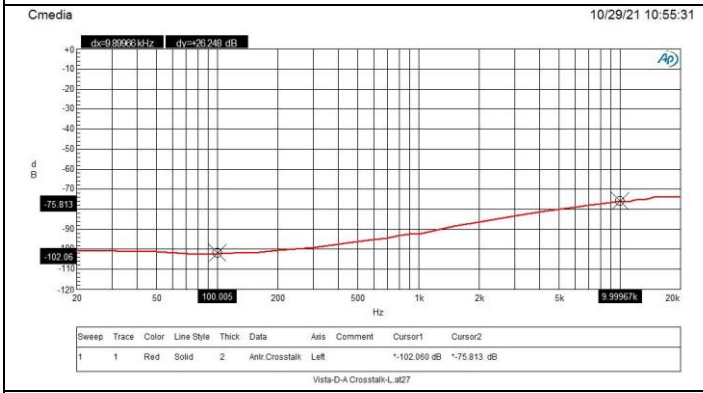
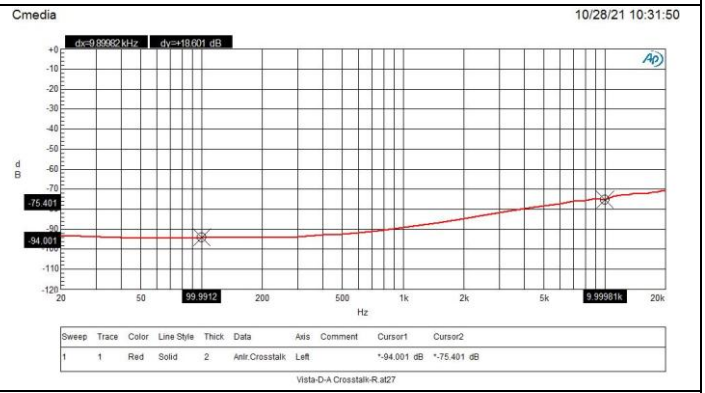
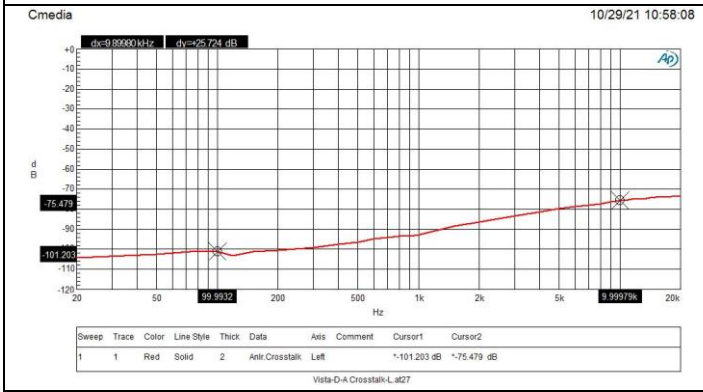
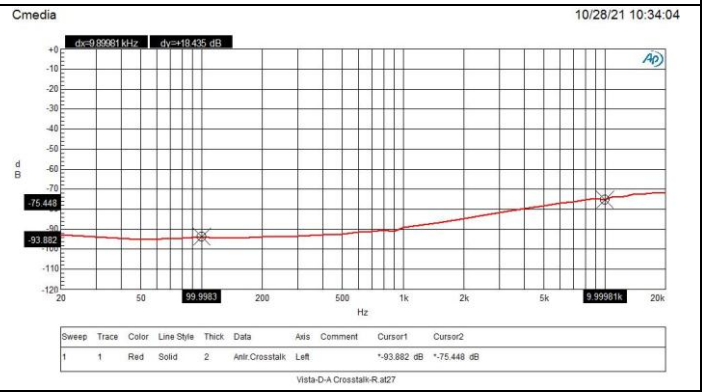
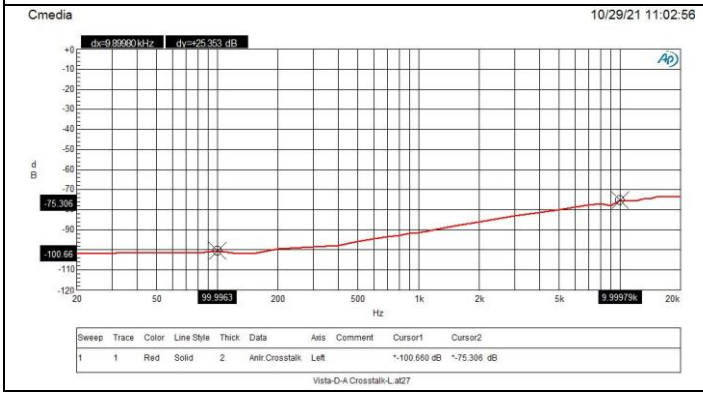
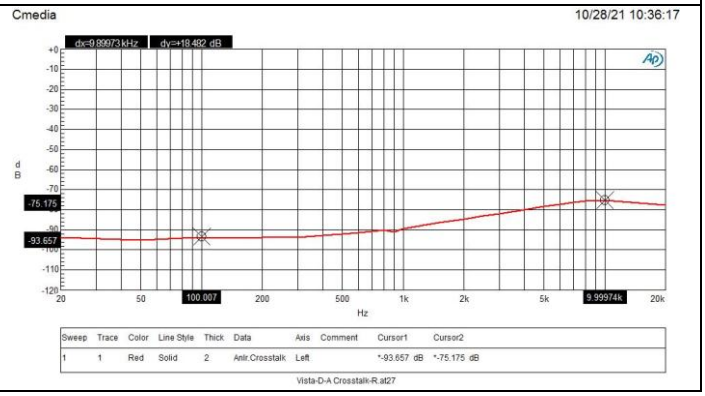
44.1K/16bits L	44.1K/16bits R
	
48K/16bits L	48K/16bits R
	
96K/24bits L	96K/24bits R
	
192K/24bits L	192K/24bits R
	

Figure 9： DAC 32Ω loading Cascade 33 Ω, Cross-talk

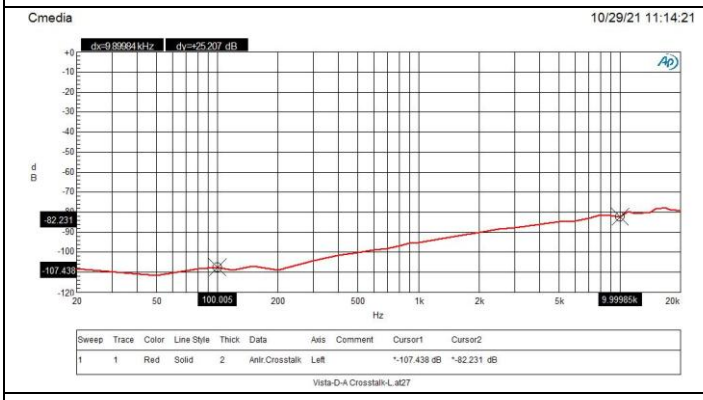
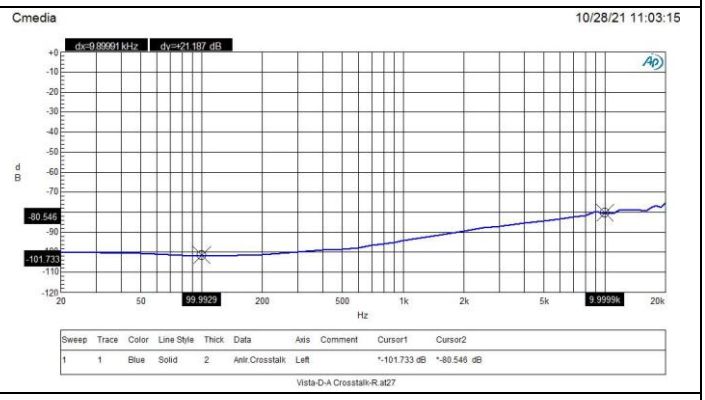
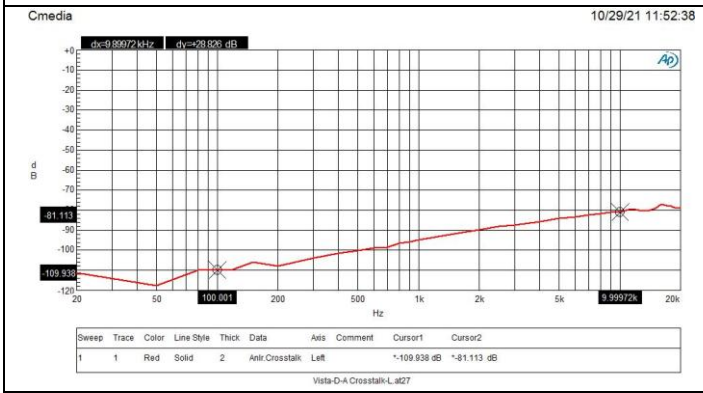
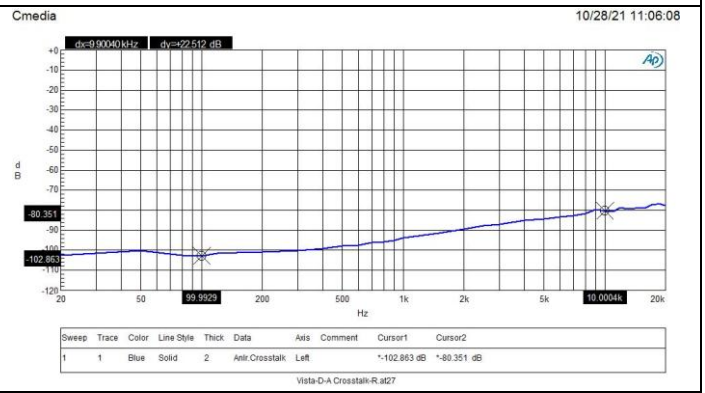
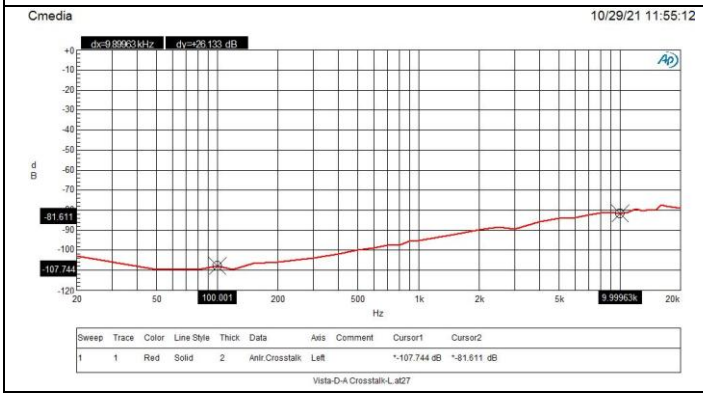
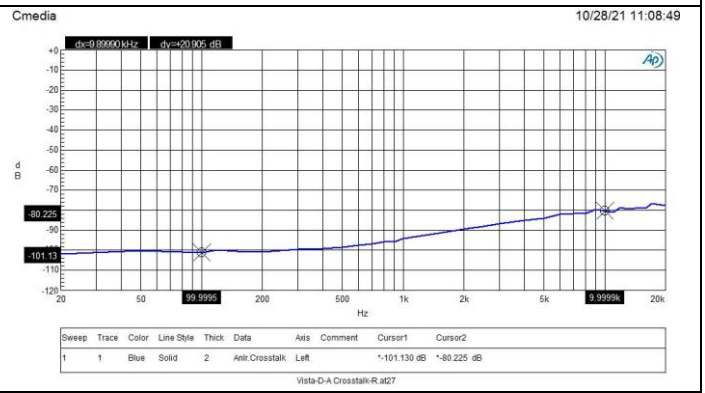
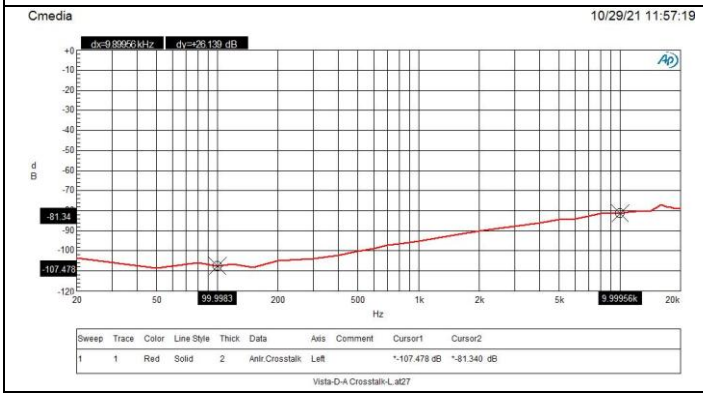
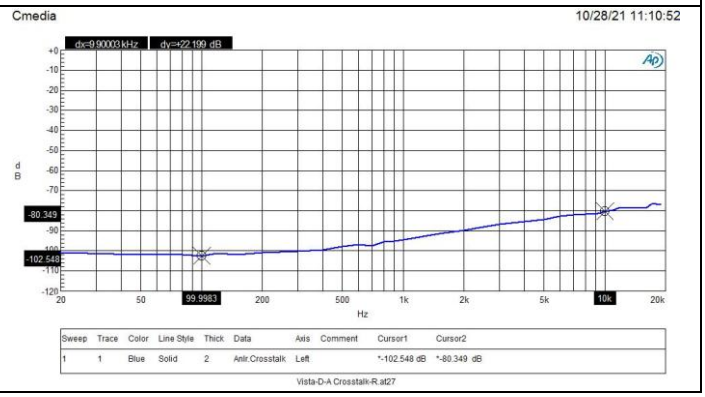
44.1K/16bits L	44.1K/16bits R
	
48K/16bits L	48K/16bits R
	
96K/24bits L	96K/24bits R
	
192K/24bits L	192K/24bits R
	

Figure 10：DAC 10KΩ loading,Frequency Response

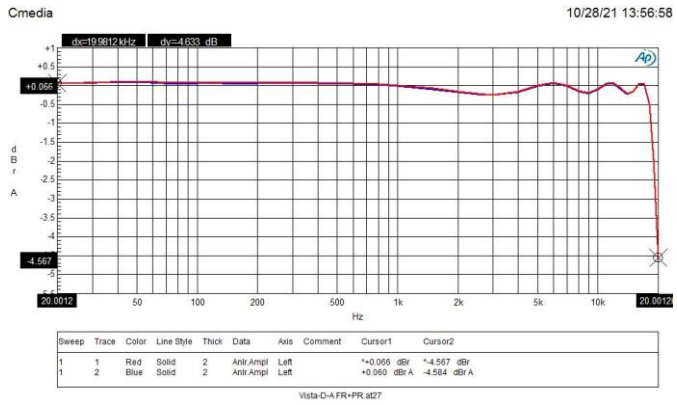
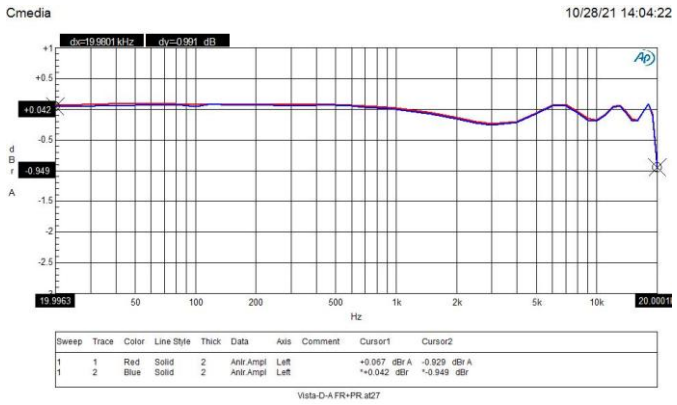
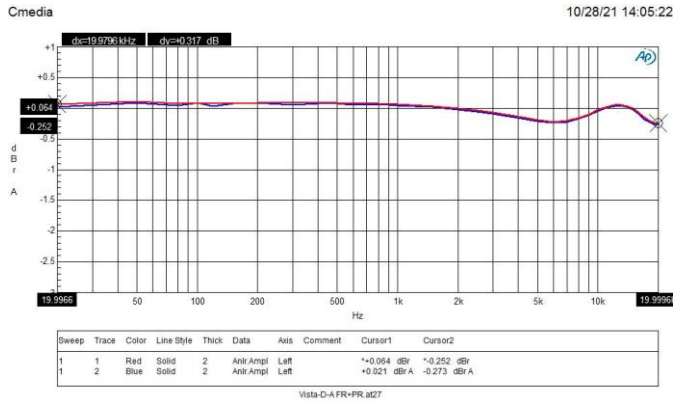
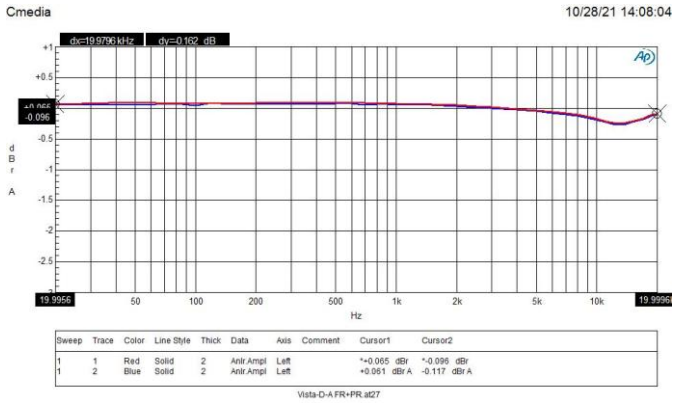
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 11：DAC 32Ω loading,Frequency Response

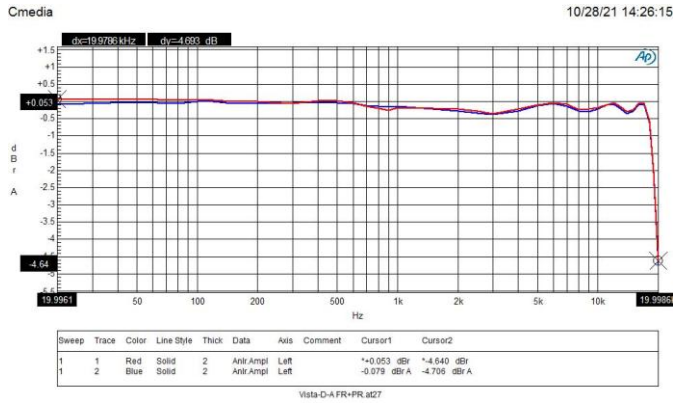
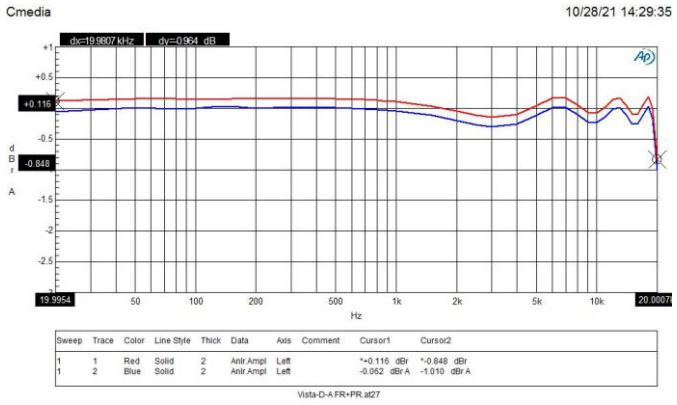
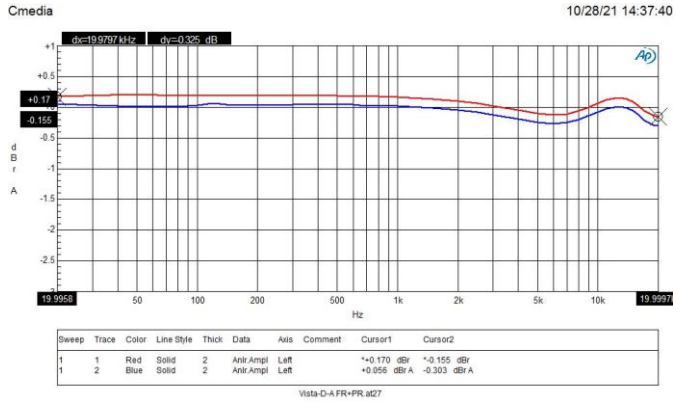
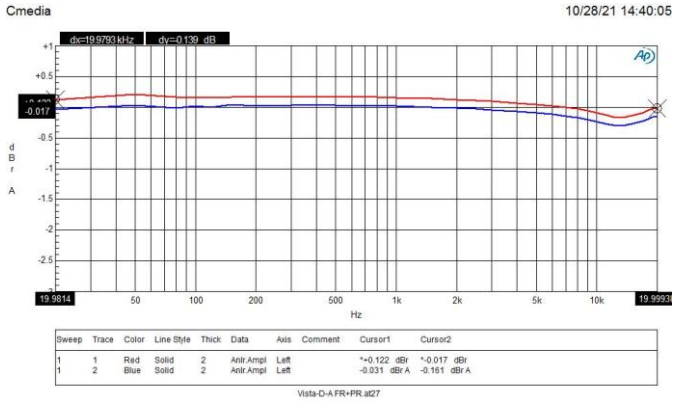
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 12：DAC 32Ω loading Cascade 33 Ω ,Frequency Response

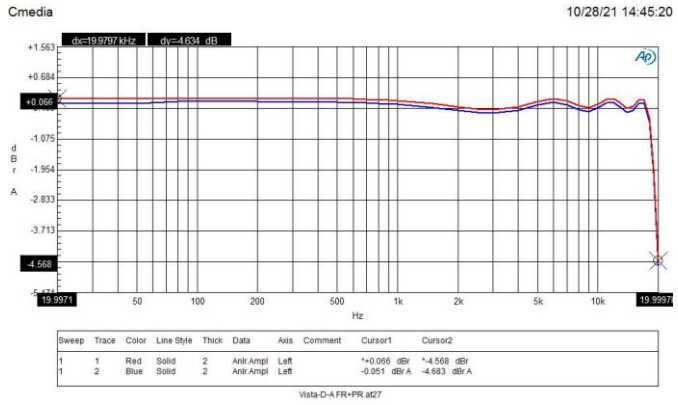
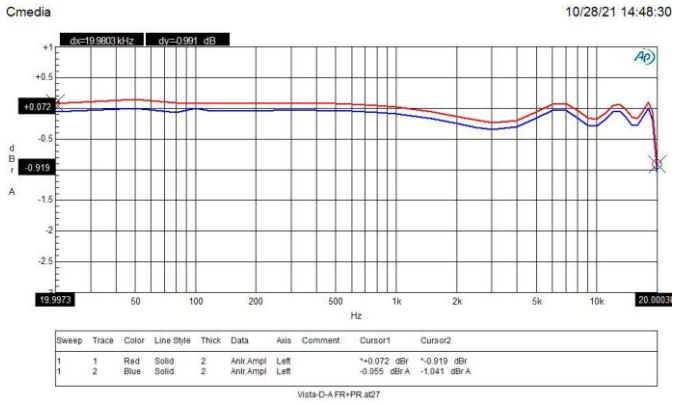
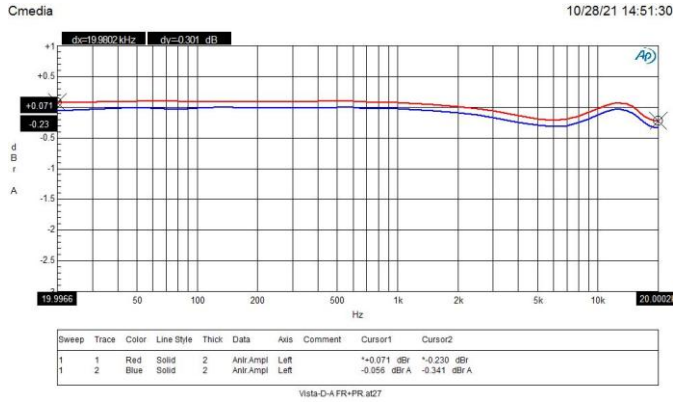
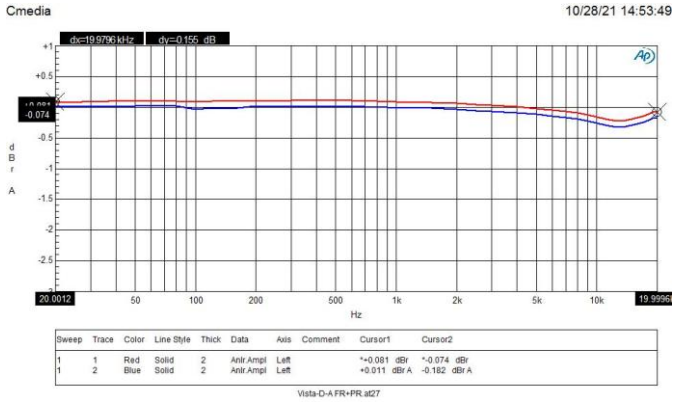
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 13：DAC 10KΩ loading, Interchannel phase delay

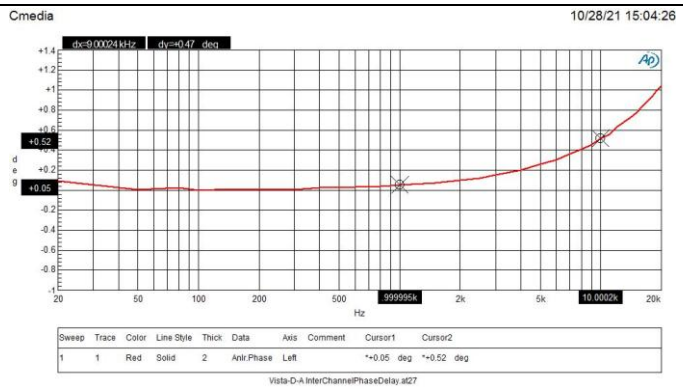
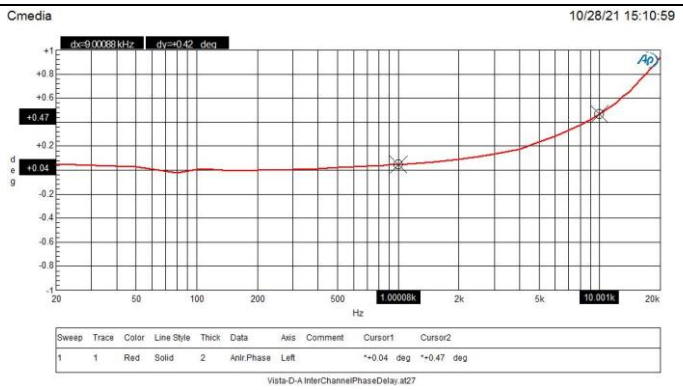
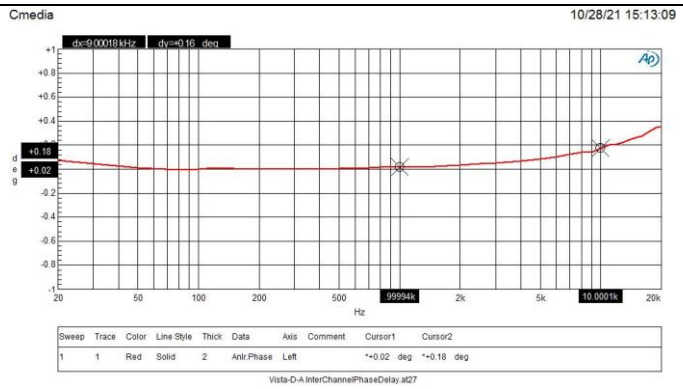
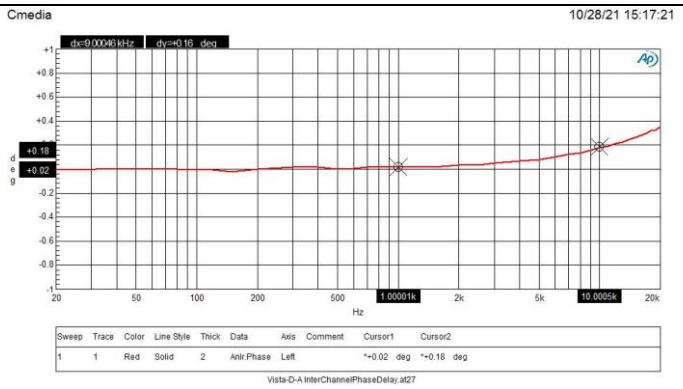
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 14：DAC 32Ω loading , Interchannel phase delay

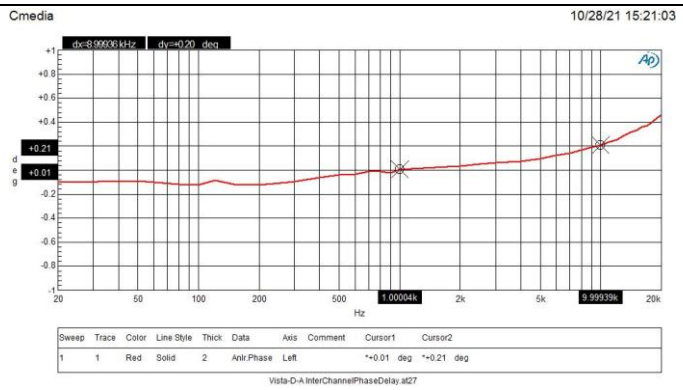
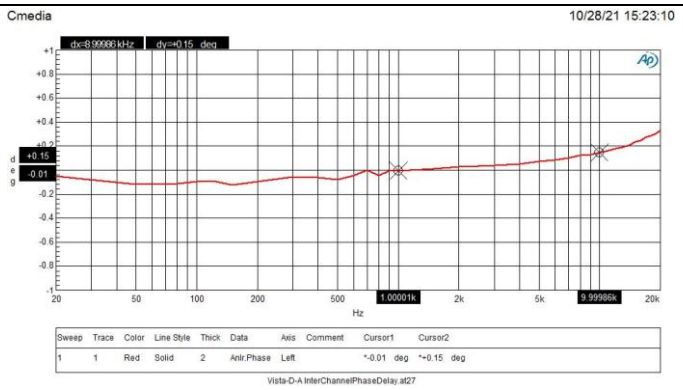
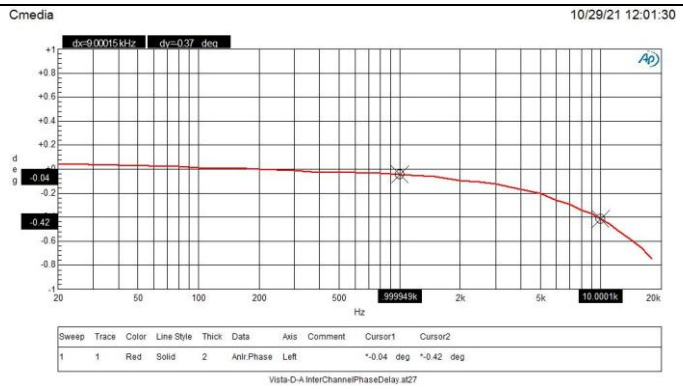
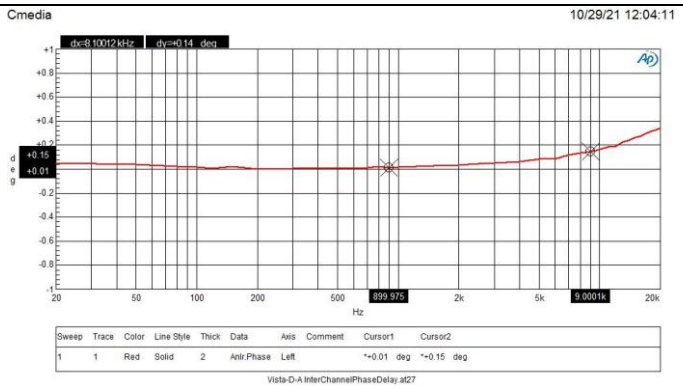
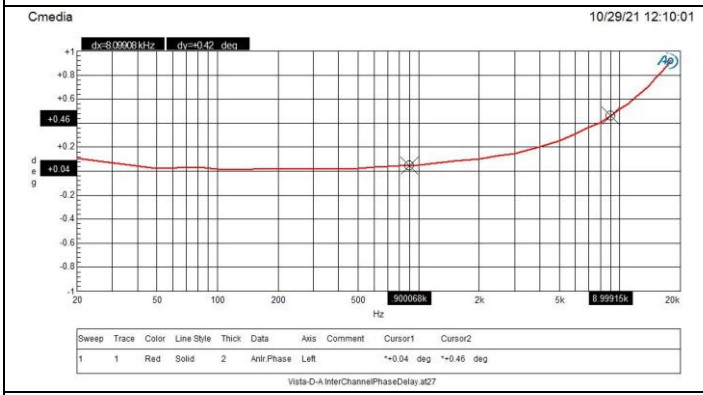
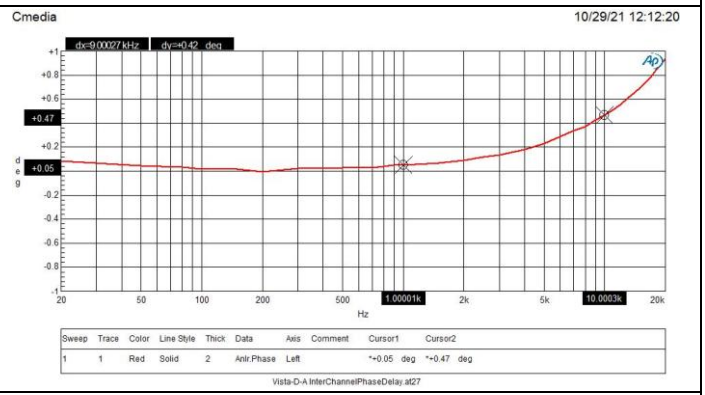
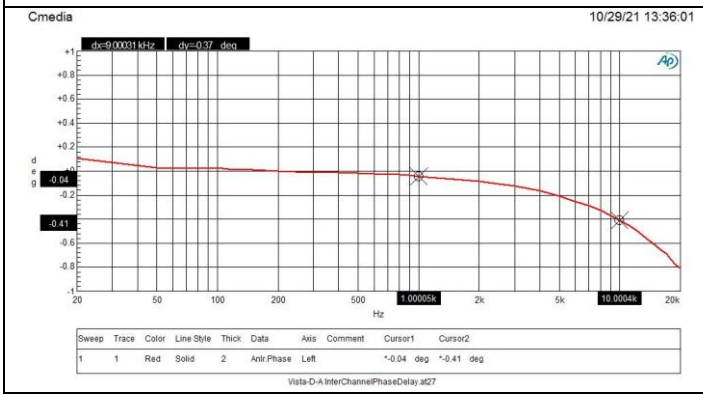
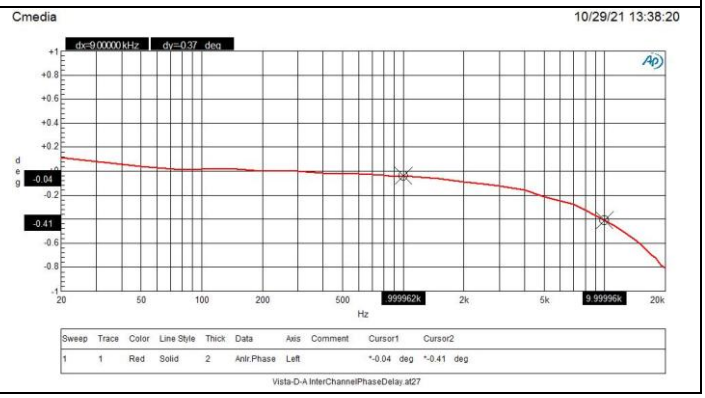
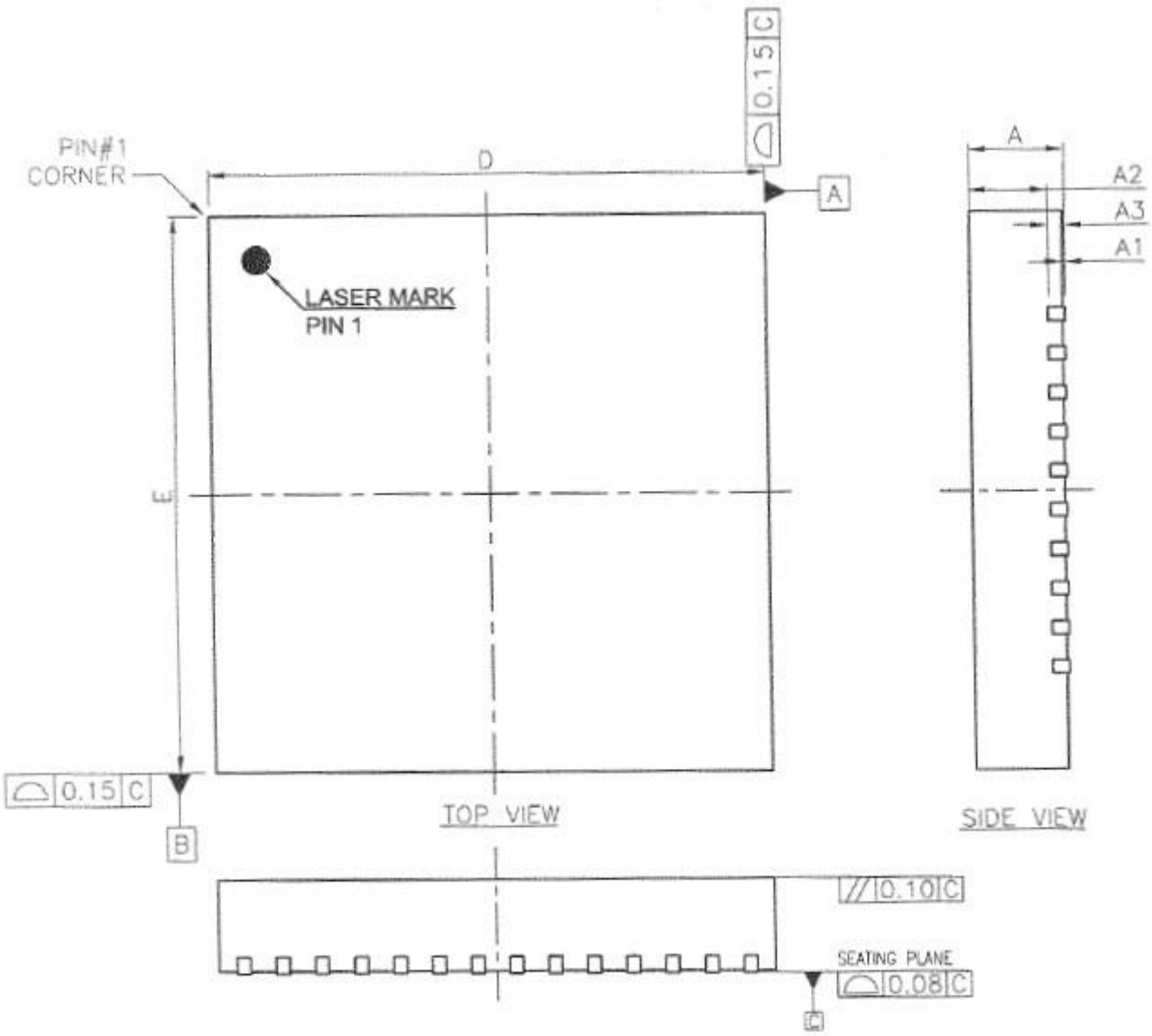
44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

Figure 15：DAC 32Ω loading Cascade 33 Ω , Interchannel phase delay

44.1K/16bits	48K/16bits
	
96K/24bits	**192K/24bits**
	

9 Package Dimensions

9.1 QFN48 5mm x 5mm (10-14-10-14)

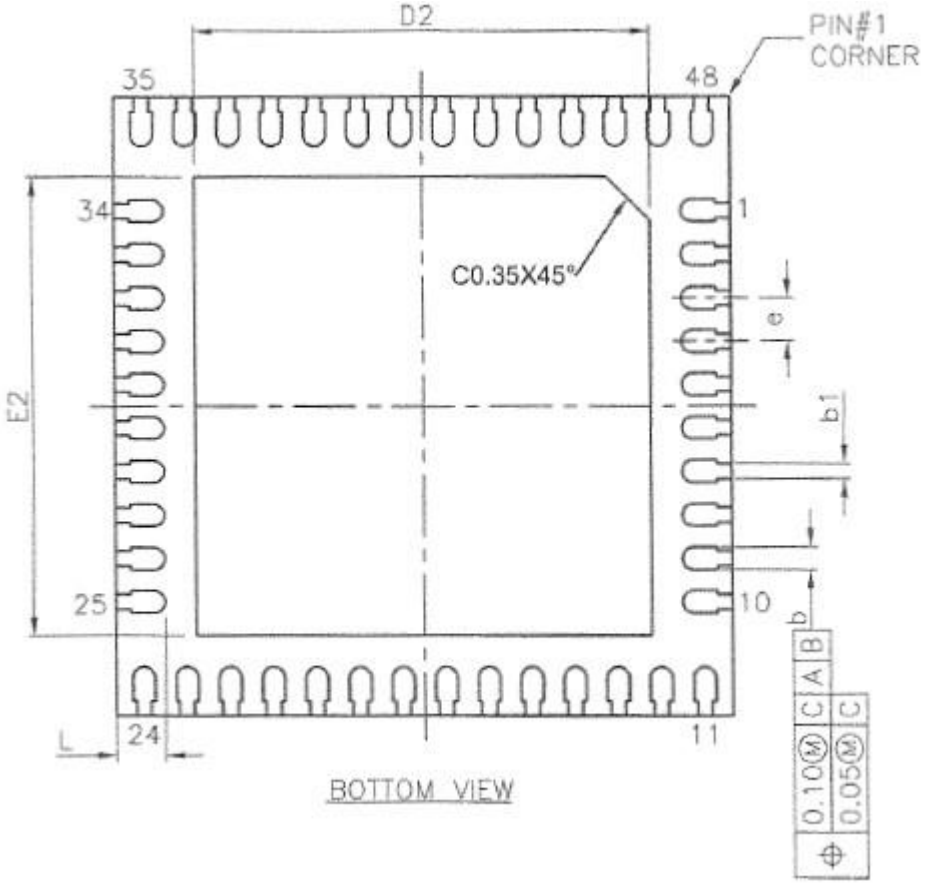


Top View

	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.65	0.70	0.75
Lead thickness	A3		0.15 REF.	
Body size	D	4.95	5.00	5.05
	E	4.95	5.00	5.05
Lead width	b	0.13	0.18	0.23
	b1	0.07	0.12	0.17
Exposed pad width	D2	3.65	3.70	3.75
Exposed pad length	E2	3.65	3.70	3.75
Lead pitch	e		0.35 BSC	
Lead length	L	0.35	0.40	0.45
Lead count	N		48L	

9.2 Recommended Land Pattern

PCB land pattern is recommended to fit the dimensions of the pad, please use the maximum value of the dimensions as reference for PCB layout. The dimensions for the ground plane are D2 by E2.



Symbol	Dimensions in mm		
	Minimum	Normal	Maximum
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
e		0.35 BSC	

Pad Size	Dimensions in mm		
	Minimum	Normal	Maximum
D2	3.65	3.70	3.75
E2	3.65	3.70	3.75
L	0.35	0.40	0.45

— End of Datasheet —

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E-MAIL：sales@cmedia.com.tw